

HP  
**KAYAK**



**HP Kayak XU800 PC Workstation**

***Technical Reference Manual***

High-Performance Desktops

PC Workstations

High-Performance



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Hewlett-Packard France  
Business Desktop Division (BDD)  
Outbound Marketing Communications  
38053 Grenoble Cedex 9  
France 1999

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## Contents

### **1 System Overview**

HP Kayak XU800 PC Workstation Overview . . . . .	9
HP Kayak XU800 PC Workstation Package . . . . .	13
Front and Side Views . . . . .	13
Rear View . . . . .	14
Internal Features . . . . .	14
Front Panel . . . . .	15
Specifications and Characteristics . . . . .	16
Physical Characteristics . . . . .	16
Electrical Specifications . . . . .	16
Power Consumption and Cooling . . . . .	17
Environmental Specifications . . . . .	18
Power Saving and Ergonometry . . . . .	19
Power Saving and Ergonometry for APM Systems . . . . .	20
Power Saving Modes and Resume Events for ACPI Systems . . . . .	20
Power-On from Space-Bar . . . . .	21
Soft Power Down . . . . .	21
Documentation . . . . .	22
Where to Find the Information . . . . .	23

---

## Contents

### 2 System Board

System Board Overview .....	28
Architectural View .....	29
Accessory Card Slots .....	30
Universal AGP Pro Slot .....	30
PCI Slots .....	31
System Board Switches .....	33
Chipset .....	34
Memory Controller Hub (8240) .....	35
Accelerated Graphics Port (AGP) Bus Interface .....	38
AGP 4x Bus .....	38
Main Memory Controller .....	39
PCI 64-bit Hub .....	44
PCI 64-bit 66 MHz Bus Interface .....	45
The Input/Output Controller Hub (82801AA) .....	48
Devices on the PCI 32-bit 33 MHz Bus .....	53
Dual Chip PCI Audio Solution .....	54
Devices on the SMBus .....	55
Devices on the Low Pin Count Bus .....	60
The Super I/O Controller (NS 87364) .....	61
FirmWare Hub (82802AB) .....	62
Host Bus .....	64
Intel Pentium III Processor .....	65
Optional Second Processor .....	65
Cache Memory .....	67
Assigned Device Interrupts .....	68
Input/Output Controller Hub Interrupts .....	68
PCI 64-bit Hub Interrupts .....	68
Interrupt Controllers .....	68

---

## Contents

### 3 Interface Cards

Graphics Cards . . . . .	71
Matrox Millennium G250 Graphics Card . . . . .	71
Matrox Millennium G400 Graphics Card . . . . .	74
3Dlabs Oxygen GVX1 . . . . .	77
ELSA Synergy II Graphics Card . . . . .	79
Network Cards . . . . .	81
HP 10/100 TX PCI LAN Interface. . . . .	81
Supported LAN Cards. . . . .	83
3COM NIC (Network Interconnect) LAN Card. . . . .	83
INTEL NIC (Network Interconnect) LAN Card . . . . .	85

### 4 Mass Storage Devices

Flexible Disk Drives . . . . .	87
Hard Disk Drives . . . . .	87
CD-ROM Drives. . . . .	88

### 5 HP BIOS

HP/NBA BIOS Summary. . . . .	91
Using the HP Setup Program . . . . .	92
Updating the System BIOS. . . . .	95
Restoring BIOS Default Settings. . . . .	95
Clearing the CMOS . . . . .	96
Clearing Passwords . . . . .	97
Recovering the BIOS (Crisis Mode) . . . . .	98
Adaptec SCSISelect Configuration Utility . . . . .	99
Default Settings. . . . .	99
Starting the SCSISelect Configuration Utility . . . . .	101
BIOS Addresses. . . . .	102
System Memory Map. . . . .	102
HP I/O Port Map (I/O Addresses Used by the System). . . . .	103

---

## Contents

DMA Channel Controllers . . . . .	104
IRQs Used by the PC Workstation . . . . .	105

### **6 Tests and Error Messages**

<b>MaxiLife Test Sequence and Error Messages . . . . .</b>	<b>107</b>
Basic Pre-boot Diagnostics . . . . .	108
Post Test Sequence and Post Error . . . . .	109
Operating System Boot Phase . . . . .	110
Run-Time Errors . . . . .	111
Main Menu . . . . .	112
<b>Order in Which POST Tests Are Performed . . . . .</b>	<b>115</b>
<b>Error Message Summary . . . . .</b>	<b>123</b>
Beep Codes . . . . .	127

### **7 Connectors and Sockets**

Rear Panel Socket Pin Layouts . . . . .	137
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## Preface

This manual is a technical reference and BIOS document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturers' proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography on the following page.

For all warning and safety instructions, refer to the user guide delivered with the PC Workstation.

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## Conventions

The following conventions are used throughout this manual to identify specific numeric elements:

Hexadecimal numbers are identified by a lower case h.  
For example, 0FFFFFFFh or 32F5h

Binary numbers and bit patterns are identified by a lower case b.  
For example, 1101b or 10011011b

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## Bibliography

Online documentation can be obtained from the HP World Wide Web site: [www.hp.com/go/kayaksupport](http://www.hp.com/go/kayaksupport).

- HP Kayak XU800 PC Workstation *User's Guide* D8369-90001<sup>1</sup> — as well as English, this guide is also available in various languages.
- HP Kayak XU800 PC Workstation *Troubleshooting Guide* — available in English, French, Italian, German, Spanish, Swedish and Japanese.
- HP Kayak XU800 PC Workstation *Technical Notes* — English only.
- HP Kayak XU800 PC Workstation *Service Handbook Chapter* — English only.
- Image Creation and Recovery CD-ROM* — 5011-6692-xx<sup>2</sup>.

### Extra Information Can Be Obtained At:

- ELSA GLoria Synergy graphics card  
<http://www.elsa.com>
- Matrox graphics cards  
<http://www.matrox.com>
- 3D Labs Oxygen GVX1 graphics card  
<http://www.3dlabs.com>
- Intel Chipsets. Intel I840 chipset  
<http://developer.intel.com>
- Intel Pentium III Processor  
<http://developer.intel.com>

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1. Also includes information about the HP Kayak XM600 Minitower PC Workstation.

2. xx = Language code.



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## System Overview

This manual describes the *HP Kayak XU800 PC Workstation* and provides detailed system specifications.

This chapter introduces the external features, and lists the specifications and characteristic data of the system. It also provides a summary of the documentation available.

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### HP Kayak XU800 PC Workstation Overview

The *HP Kayak XU800 PC Workstation* is based on the Extended ATX (E-ATX) form factor.

The following table provides an overview of the system.

Feature	Description
<i>System Board</i>	E-ATX with a dimension of 12.8-inch x 11.4-inch.
<i>Processor</i>	All models have support for up to two Intel Pentium® III processors. For Processor 1, a VRM (Voltage Regulator Module) is integrated on the system board, while there is a VRM socket for a second processor.
<i>Cache Memory (integrated in processor package)</i>	<ul style="list-style-type: none"><li>• Level-One: 16 KB code, 16 KB data.</li><li>• Level-Two: 256 KB.</li></ul>
<i>Internal CPU Clock Rate External Processor Bus</i>	533 MHz, 600 MHz, 667 MHz, 733 MHz, 800 MHz and higher. 133 MHz Front Side Bus.
<i>Chipset</i>	Intel® Chipset (I840) including, Input/Output Controller Hub (ICH), PCI 64-bit Hub (P64H), FirmWare Hub (FWH) and Memory Repeater Hub (MRH-S) for SDRAM support.
<i>Super I/O Chip</i>	NS 87364.
<i>BIOS (Basic Input/Output System)</i>	Based on the core of AMIBIOS, including: <ul style="list-style-type: none"><li>• 4 M/bits of flash memory.</li><li>• Support for PCI 2.2 Specification.</li><li>• Support for RDRAM or SDRAM memory modules.</li></ul>
<i>Firmware - BIOS</i>	Flash EEPROM: Intel's Firmware hub concept.

## 1 System Overview

### HP Kayak XU800 PC Workstation Overview

Feature	Description
<i>HP MaxiLife Utility (available on all models)</i>	Hardware monitoring utility that monitors system components via the I <sup>2</sup> C bus and a LCD status panel.
<i>Operating System</i>	All models are preloaded with Windows NT <sup>®</sup> 4.0 SP5.
<i>Main Memory Maximum amount of memory that can be installed is: 2 GB (4 x 512 MB)</i>	Models include either: <ul style="list-style-type: none"><li>• Four RIMM sockets supporting RDRAM ECC memory modules installed in <i>pairs</i>. Any unused RIMM sockets must contain a continuity module. Models are supplied with either 128 MB or 256 MB RDRAM ECC main memory installed in <i>pairs</i>. Memory upgrades are available in <i>pairs</i> of: 64 MB, 128 MB, 256 MB or 512 MB RDRAM ECC modules.</li><li>• Four DIMM sockets supporting SDRAM 100 MHz ECC memory modules installed in <i>pairs</i>. Models are supplied with 128 MB of SDRAM unbuffered ECC main memory. Memory upgrades are available in <i>pairs</i> of: 64 MB, 128 MB, 256 MB or 512 MB unbuffered 100 MHz ECC SDRAM modules.</li></ul>
<i>Mass Storage</i>	Seven shelves supporting: <ul style="list-style-type: none"><li>• Two front-access, third-height 3½-inch (one for the floppy disk drive and one free) (height 1");</li><li>• Three front-access, half-height, 5¼-inch drives (height 1.0"); Possibility of installing a 3½-inch hard disk drive in one of the 5¼-inch shelves.</li><li>• Two internal 3½-inch hard disk drives (height 1.0").</li></ul>
<i>SCSI Controller</i>	Ultra 160 SCSI controller: Adaptec <sup>®</sup> AIC-7892 Ultra 160 16-bit integrated SCSI controller (160 MB/s). The internal SCSI connectors allow for up to five internal devices to be connected. Additional devices can be added outside the PC Workstation by connecting directly to the rear panel SCSI connector. The external connector allows up to ten external devices to be connected. This gives a maximum of 15 (internal + external) devices that can be connected.
<i>IDE Controller</i>	All models include an integrated Ultra ATA-66 controller that supports up to four IDE devices.

Feature	Description
<i>Video Controllers</i>	<p>Models include either:</p> <ul style="list-style-type: none"> <li>• ELSA GLoria Synergy® II AGP video controller with 32 MB of installed SGRAM video memory (maximum configuration).</li> <li>• Matrox® Millennium G250 AGP video controller with 8 MB SGRAM video memory which can be upgraded to 16 MB.</li> <li>• Matrox Millennium G400-Dual monitor AGP video controller with 16 MB SGRAM video memory (maximum configuration).</li> <li>• 3Dlabs Oxygen® GVX1, 32 MB SGRAM video memory (maximum configuration).</li> </ul>
<i>Accessory Card Slots</i>	<p>All models have:</p> <ul style="list-style-type: none"> <li>• One Universal AGP Pro 4X 50 W 32-bit slot. The AGP bus provides a high performance graphics interface.</li> <li>• Three 32-bit 33 MHz PCI<sup>1</sup> slots: 1, 2 and 5 (5 V).</li> <li>• Two 64-bit 66 MHz PCI slots: 3 and 4 (3.3 V).</li> </ul> <p>The majority of the configurations are delivered with PCI slots 1 to 4 vacant.</p>
<i>LAN Card</i>	<p>All models are supplied with an HP 10/100BT PCI Ethernet Adapter LAN card installed in PCI slot 5, supporting Wake-On LAN (WOL) and PCI 2.2 Specification.</p>
<i>CD-ROM Drive</i>	<p>Models include either an IDE 48X CD-ROM, CD-RW drive or DVD drive.</p>
<i>Audio</i>	<p>Integrated on the system board CS4280 audio PCI chip and AC97 Codec (CS4297) audio.</p>
<i>HP UltraFlow Cooling System</i>	<p>Cooling system with multiple temperature-regulated fans to optimize cooling. Alert reporting to MaxiLife and TopTools.</p>

1. All five PCI slots comply with the PCI Specification 2.2.

## 1 System Overview

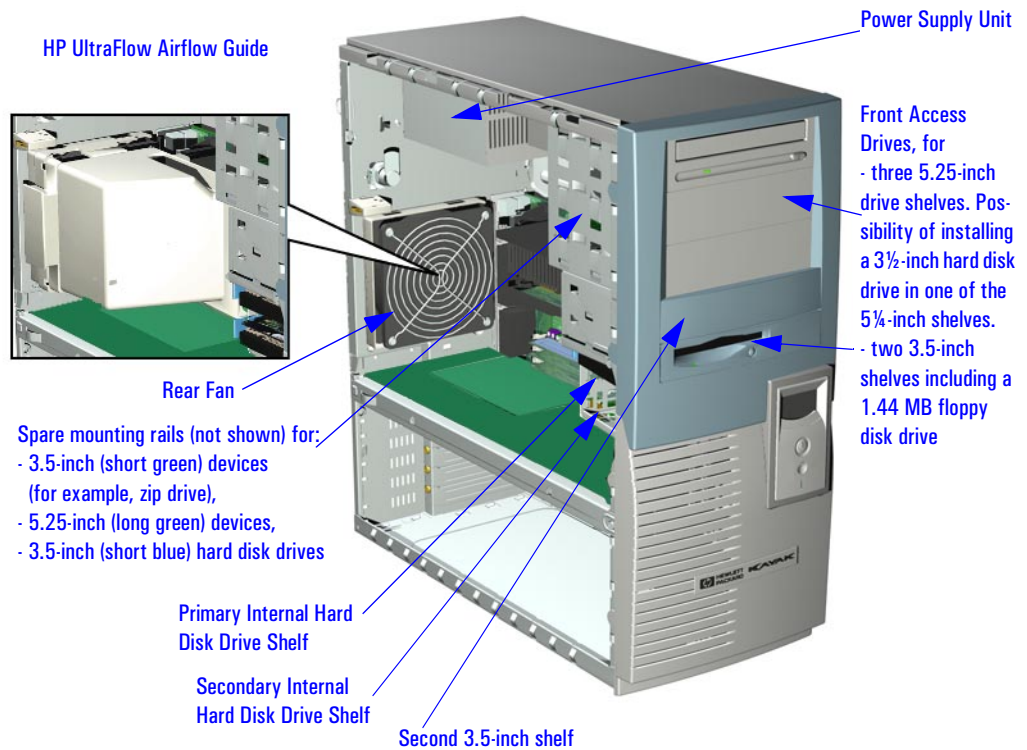
### HP Kayak XU800 PC Workstation Overview

Feature	Description
<b><i>System Board Connectors</i></b>	<ul style="list-style-type: none"><li>• One flexible disk drive connector</li><li>• Two ATA-66 IDE connectors (for up to four IDE devices)</li><li>• One 16-bit Ultra 160 SCSI connector and one SCSI terminator. The SCSI cable is routed from the SCSI connector on the system board (located near the system switches) to the SCSI devices inside the chassis, onto an onboard SCSI terminator (behind the processor), and finally onto the external SCSI connector on the rear panel. The onboard SCSI terminator is automatically deactivated when an external device is attached.</li><li>• One CD-IN audio connector</li><li>• AUX connector</li><li>• Internal speaker connector</li><li>• One WOL connector</li><li>• One status panel connector</li><li>• Two power supply connectors that must be connected</li><li>• Two fan connectors (one for the PCI fan, and one for the rear fan)</li><li>• One battery socket</li></ul> <p>The system board layout with all connectors can be found on <a href="#">page 28</a>.</p>
<b><i>Rear Panel Connectors (color coded)</i></b>	<ul style="list-style-type: none"><li>• 9-pin serial (two, buffered)<ul style="list-style-type: none"><li><input type="checkbox"/> Standard: Two UART 16550 buffered serial ports (both RS-232-C).</li><li><input type="checkbox"/> Serial Ports A and B: 2F8h (IRQ 3), 2E8h (IRQ 3), 3F8h (IRQ 4), 3E8h (IRQ 4), or Off— (if one port uses 2xxh, the other port must use 3xxh).</li></ul></li><li>• Dual USB connectors</li><li>• External 16-bit U160m SCSI connector</li><li>• Audio<ul style="list-style-type: none"><li><input type="checkbox"/> Joystick/Dual MIDI connector</li><li><input type="checkbox"/> LINE IN jack (3.5 mm)</li><li><input type="checkbox"/> LINE OUT jack (3.5 mm)</li><li><input type="checkbox"/> MIC IN jack (3.5 mm)</li></ul></li><li>• Keyboard/Mouse<ul style="list-style-type: none"><li><input type="checkbox"/> HP enhanced keyboard with mini-DIN connector</li><li><input type="checkbox"/> HP enhanced scrolling mouse with mini-DIN connector</li></ul></li><li>• 25-pin parallel connector<ul style="list-style-type: none"><li><input type="checkbox"/> Mode: Centronics or bidirectional modes (ECP/EPP)</li><li><input type="checkbox"/> Parallel port: 1 (378h, IRQ 7), 2 (278h, IRQ 5), or Off.</li></ul></li></ul>

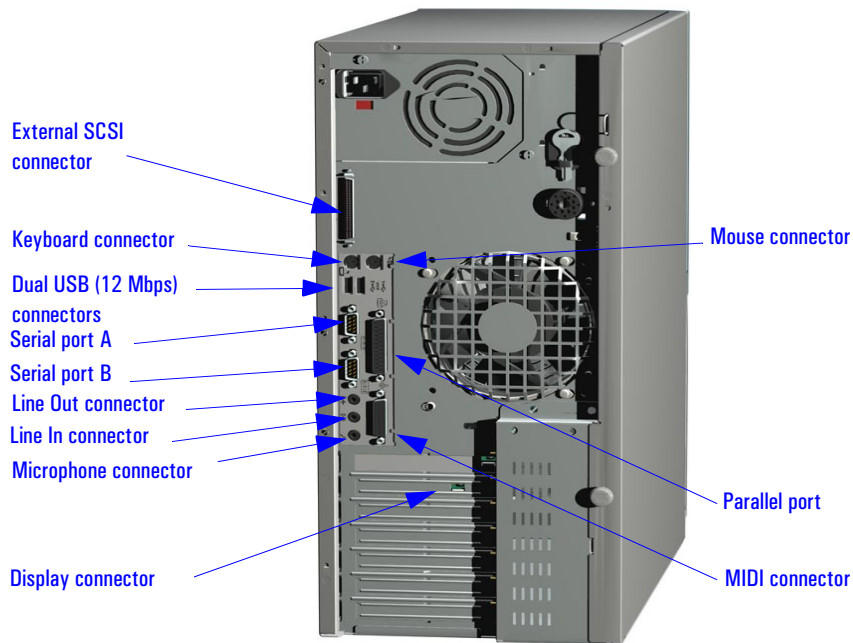
## HP Kayak XU800 PC Workstation Package

The following two diagrams show the front and rear views of the *HP Kayak XU800 PC Workstation*.

### Front and Side Views



#### Rear View



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### Internal Features

The core architecture of the *HP Kayak XU800 PC Workstation* is constructed around: Memory Controller Hub (MCH), Input/Output Controller Hub (ICH), FirmWare Hub (FWH) and the Host bus.

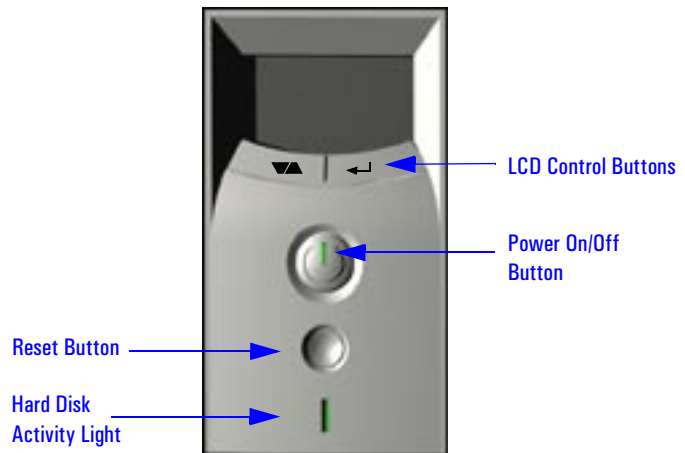
The *HP Kayak XU800 PC Workstation* can support up to two Pentium III processors. This processor is described on [page 65](#).

The components of the system board are described in [chapter 2](#); the characteristics of the PC Workstation's video and storage devices are described in [chapter 3](#); mass storage devices are described in [chapter 4](#); the HP BIOS routines are summarized in [chapter 5](#); and the Power-On Self-Test routines are described in [chapter 6](#).

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## Front Panel

The front panel of *HP Kayak XU800 PC Workstation* has the following features:



- *Liquid Crystal Display (LCD)*. LCD error messages and available menus are described on [page 107](#).
- *On/Off LED*. There are five states:
  - Blank. Indicates that the computer is turned off.
  - Green**. Indicates that the computer is turned on and running correctly.
  - Red**. Indicates that there is a Power-On Self-Test (POST) error.
  - Red flashing**. Indicates that there is a MaxiLife (Diag/Alarm) error.
  - Amber**. Displayed during system reset, system lock, Standby mode (Windows 98) or Suspend mode (Windows 95).
- *Hard disk drive activity LED*. Activated during POST and when the hard disk drive is being accessed.

## Specifications and Characteristics

### Physical Characteristics

System Processing Unit	
Weight (excl. keyboard and display):	14.4 kilograms (31.68 pounds)
Dimensions:	47.0 cm max. (D) by 21,0 cm (W) by 49.0 cm (H) (18.50 inches by 8.26 inches by 19.29 inches)
Footprint:	0.09 m <sup>2</sup> (1.06 sq ft)

### Electrical Specifications

Parameter	Total Rating		Peak (15 secs.)	Maximum per PCI Slots <sup>1</sup> (1,2 & 5) 32-bit 33 MHz	Maximum per PCI Slots <sup>1</sup> (3 & 4) 64-bit 66 MHz	Maximum for Universal AGP Pro Slot <sup>2</sup>
Input voltage - Switch select	100 - 127 VAC	200 - 250 V Vac	—	—	—	—
Input current (max)	9 A	4.5 A	—	—	—	—
Input frequency	50 to 60 Hz		—	—	—	—
Available power	300 W		320 W	100 W for PCI slots and AGP Pro slot		
Max current at +12 V	13.5 A		15 A	0.5 A	0.5 A	9.2 A
Max current at -12 V	0.8 A		—	0.1 A	0.1 A	—
Max current at +3.3 V	1.5 A		—	7.6 A	7.6 A	I <sub>max</sub> (V <sub>cc</sub> ) = 7.6 A
Max current at V <sub>ddq</sub> (3.3 V or 1.5 V)	—		—	—	—	I <sub>max</sub> (V <sub>ddq</sub> ) = 2 A
Max current at +5 V	32 A		—	5 A	5 A	2 A
Max current at -5 V	0.5 A		—	—	—	—
Max current at +5V <sub>stdby</sub> <sup>3</sup> combined with 3.3 V stdby	2 A		—	1.5 A total on 3.3 V stdby		

1. The maximum power dissipation for a PCI card is 25 W (refer to PCI specifications 2.2 on [page 31](#)).
2. An AGP Pro card uses the electrical and cooling resources of both the Universal AGP Pro slot and the adjacent PCI slot. Power limitation is managed in the BIOS.
3. Refer to System Board Switch 10 on [page 33](#).



Some examples of a supported configuration with combined power consumption of 100 W (PCI slots + Universal AGP Pro slot):

Number of PCI Accessory Cards	AGP Pro Slot	Accessory Card Power Consumption	Total Power Supply Used
Four	One AGP Pro Card (50 W)	1 x 5 W PCI accessory card + 3 x 15 W PCI accessory cards + 0 W empty PCI slot (adjacent to Universal AGP Pro slot) + 1 x 50 W AGP Pro card	100 W
Four	One AGP Pro Card (50 W)	1 x 5 W PCI accessory card + 1 x 15 W PCI accessory card + 2 x 12.5 W PCI accessory cards + 0 W empty PCI slot (adjacent to Universal AGP Pro slot) + 1 x 50 W AGP Pro card	100 W
Five	One AGP Standard Card (25 W)	1 x 5 W PCI accessory card + 2 x 25 W PCI accessory cards + 2 x 10 W PCI accessory cards + 1 x 25 W AGP standard card	100 W

An attempt to draw too much current (such as a short circuit across edge-connector pins, or an accessory board that is not suitable for this PC Workstation), will cause the overload protection in the power supply to be triggered, and will shut down the PC Workstation.

**NOTE**

When the PC Workstation is turned off with the power button on the front panel, the power consumption falls below the low power consumption (refer to the following table), but is not zero. The special on/off method used by this PC Workstation extends the lifetime of the power supply. To reach zero power consumption in “off” mode, either unplug the PC Workstation from the power outlet or use a power block with a switch.

**Power Consumption and Cooling**

The power consumption and acoustics (shown in the Environmental Specifications table) are valid for a standard configuration as shipped (one processor, 256 MB of memory, 300 W power supply, one hard disk drive, video card, LAN card).

All information in this section is based on primary power consumptions.

Power consumption - Windows NT:	230 V / 50 Hz	115 V / 60 Hz
• Operating with input/output (disk access)	85.5 W - 291.7 Btu/h <sup>1</sup>	84.5 W - 288.3 Btu/h
• Operating without input/output (idle)	75.8 W - 258.6 Btu/h	77.2 W - 263.4 Btu/h
• Off with LAN card	4.2 W - 14.3 Btu/h	4 W - 13.6 Btu/h

<sup>1</sup>. 1 W = 3.4121 Btu/h

## 1 System Overview

### Specifications and Characteristics

Component:	
<ul style="list-style-type: none"> <li>• Processor:</li> <li>• SCSI HDD with access:</li> <li>• SCSI HDD with no access:</li> <li>• PCI card:</li> </ul>	50 W - 170.6 Btu/h 23 W - 78.4 Btu/h 16 W - 54.5 Btu/h 10 W - 36 W - 34.1 Btu/h - 122.8 Btu/h

## Environmental Specifications

Environmental Specifications (System Processing Unit, with Hard Disk)		
Operating Temperature	+10 °C to +35 °C (+50 °F to +95 °F)	
Storage Temperature	-40 °C to +70°C (-40 °F to +158 °F)	
Operating Humidity	15% to 85% (relative) <sup>1</sup>	
Storage Humidity	8% to 85% (relative) <sup>1</sup>	
Acoustic noise emission (as defined ISO 7779):	<b>Sound Power</b>	<b>Sound Pressure</b>
<ul style="list-style-type: none"> <li>• Operating</li> <li>• Operating with hard disk access</li> <li>• Operating with floppy disk access</li> </ul>	LwA < = 43.9 dB	LpA < = 30.8 dB
	LwA < = 44.9 dB	LpA < = 31.8 dB
	LwA < = 46.7 dB	LpA < = 33.6 dB
Operating Altitude	10000 ft (3100m) max	
Storage Altitude	15000ft (4600m) max	

<sup>1</sup>non condensing conditions.

Operating temperature and humidity ranges may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity levels can aggravate static electricity problems and cause excessive wear of the disk surface.

## Power Saving and Ergonometry

Depending on the operating system, the following power management types are available:

- *No sleeping state*: Windows NT 4 (Full On and Off).
- *APM*: Windows 95 and Windows 98 SE APM (Full On, Standby, Suspend and Off).
- *ACPI*: Windows 98 SE ACPI and Windows 2000 (Full On, S1, Suspend to RAM, Suspend to disk, Off).

		Windows 2000	Windows 98 SE	Windows NT 4	Windows 95
<b>A P M</b>	<i>Full On</i>	Not Supported by Windows 2000	Supported	Supported	Supported
	<i>Standby</i>		Supported	Not Supported by Windows NT 4	Supported
	<i>Suspend</i>		Supported	Not Supported by Windows NT 4	Supported
	<i>Off</i>		Supported	Supported	Supported
<b>A C P I</b>	<i>S1 (processor stopped)</i>	Supported	Supported	APM only Operating System	
	<i>S3<sup>1</sup> (suspend to RAM)</i>	Supported	Supported		
	<i>S4 (suspend to disk / hibernation)</i>	Supported	Not Supported by Windows 98		
	<i>S5 (off)</i>	Supported	Supported		

<sup>1</sup>. It is anticipated that the S3 feature will be supported by HP Windows 2000 models. More information about this feature will be documented with the HP Windows 2000 release.

## 1 System Overview

### Power Saving and Ergonometry

#### Power Saving and Ergonometry for APM Systems

	Full On	Standby <sup>1</sup>	Suspend <sup>1</sup>	Off
<b>Processor</b>	Normal speed	Normal speed	Halted	Halted
<b>Display</b>	On	Blanked, < 30 W, on models with integrated graphics	Blanked, < 5 W (typ)	Blanked, < 5 W (typ)
<b>Hard disk drive</b>	Normal speed	Stopped	Halted	Halted
<b>Power consumption</b>	supports up to 300 W	< 40 W (230V, 50 Hz) < 27 W (115V, 60 Hz)	< 40 W (230V, 50 Hz) < 21 W (115V, 60 Hz)	(plugged in but turned off) < 5 W (average)
<b>Resume events</b>		Keyboard, mouse, alarms, LAN, modem, USB	Keyboard, network (RWU), modem, USB	Space bar or power button, RPO
<b>Resume delay</b>		Instantaneous	a few seconds	Boot delay

<sup>1</sup>. Not supported by Windows NT 4.

#### Power Saving Modes and Resume Events for ACPI Systems

	Full On	S1	Suspend to RAM	Suspend to Disk	Off
<b>Processor</b>	Normal speed	Halted	Off	Off	Off
<b>Display</b>	On	Blanked	Off	Off	Off
<b>Hard Disk Drive</b>	Normal speed	Halted	Off	Off	Off
<b>Active Power Planes</b>	VCC VCCAux	VCC VCCAux	Memory VCCAux	VCCAux	VCCAux
<b>Power Consumption</b>	Supports up to 300 W	< 40 W	< 10 W	< 10 W	< 10 W
<b>Resume Events</b>		Power button, LAN, Modem, USB, Scheduler, HP Start Key	Power button, LAN, Modem, Scheduler, HP Start Key	Power button, LAN, Modem, Scheduler, HP Start Key	Power button, HP Start Key
<b>Resume Delay</b>		Instantaneous	Instantaneous	BIOS boot delay	Regular boot delay

### Power-On from Space-Bar

The *power-on from the space-bar* function is enabled provided that:

- The computer is connected to a Power-On keyboard (recognizable by the Power-On icon on the space bar).
- The function has been enabled by setting SW-7 to **up** (default setting) on the system board switches.
- The function has been enabled in the “Power” menu of the *Setup* program (default configuration).

### Soft Power Down

When the user requests the operating system to shut down, the environment is cleared, and the computer is powered off. *Soft Power Down* is available with the Windows NT operating system.

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## Documentation

The table below summarizes the availability of the documentation that is appropriate to the *HP Kayak XU800 PC Workstation*. Only selected publications are available in paper-based form. Most are available as printable files from the HP division support servers, or from the HP website.

Title	Division Support Server	Online at HP WWW Site (see address below)	Paper-based
<i>HP Kayak XU800 User's Guide</i>	PDF file	PDF file	Shipped with the PC Workstation <sup>1</sup>
<i>HP Kayak XU800 Troubleshooting Guide</i>	PDF file <sup>2</sup>	PDF file	No
<i>HP Kayak XU800 Training Module</i>	CD-ROM	No	No
<i>HP Kayak XU800 Technical Reference Manual</i>	PDF file (this document)	PDF file	No
<i>HP Kayak XU800 Service Handbook Chapter</i>	PDF file	PDF file	When available, it will be included in the fourth edition of the Service Handbook
<i>HP Kayak XU800 Technical Notes</i>	PDF file	PDF file	No

<sup>1.</sup> Refer to the Service Handbook Chapter for the availability of the localized monolingual and multilingual *User's Guides*.

<sup>2.</sup> Also available in French, Italian, German, Spanish, Swedish and Japanese.

### Access HP World Wide Web Site

Additional online support documentation, BIOS upgrades and drivers are available from HP's World Wide Web site, at the following address:

World-Wide Web URL: <a href="http://www.hp.com/go/kayaksupport">http://www.hp.com/go/kayaksupport</a>
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then select HP Kayak XU800 PC Workstation.

## Where to Find the Information

The table below summarizes the availability of information within the *HP Kayak XU800 PC Workstation* documentation set.

	User's Guide	Troubleshooting Guide <sup>1</sup>	Training Module	Service Handbook	Technical Information	Technical Reference Manual
<b>Introducing the PC</b>						
<i>Product features</i>	Standard configuration.		New features.	Exploded view. Parts list.	Configuration.	Key features.
<i>Product model numbers</i>				Product range. CPL dates.		
<i>Environmental</i>	Setting up the PC. Working in comfort.					
<i>Safety Warnings</i>	Electrical, multimedia, safety, unpacking, removing & replacing cover.	Safety.				
<i>Finding on-line information</i>	Preloaded, HP Web sites.	HP Web sites.	HP Web sites.		HP Web sites.	HP Web sites, others.
<i>Technical information</i>	Basic details.		Basic details.		Advanced.	Advanced.
<i>Formal documents</i>	Certificate of Conformity. Software License agreement.					
<b>Using the PC</b>						
<i>Connecting devices and turning on</i>	Rear panel connectors, starting and stopping.					
<i>BIOS</i>	Basic details.	Updating and recovering.	New features.		Memory maps.	Technical details. Memory maps.
<i>Fields and their options within Setup</i>	Basic details. Viewing <i>Setup</i> screen, using, passwords	Basic details.	New fields.			Complete list.
<i>Manageability</i>	Power management, Software and drivers.					

	User's Guide	Troubleshooting Guide <sup>1</sup>	Training Module	Service Handbook	Technical Information	Technical Reference Manual
<b>Upgrading the PC</b>						
<i>Opening the PC</i>	Full description.		New procedures.			
<i>Supported accessories</i>			Full PN details	Full PN details		
<i>Installing accessories</i>	Processor(s), memory, accessory boards, mass storage devices.	Error messages, problem solving.	New procedures.			
<i>Configuring devices</i>	Installing devices	Installing devices.			Network connection.	
<i>System board</i>	Installing and removing, connectors and switch settings.	Switch settings.	Jumpers, switches, connectors and replacing.	Jumpers, switches and connectors.	Layout and switch settings.	Jumpers, switches and connectors. Chip-set details.
<b>Repairing the PC</b>						
<i>Troubleshooting</i>	Basic, MaxiLife, hardware diagnoses.	MaxiLife, hardware diagnoses and suggested solutions.	Repair policy.	Service notes.		Advanced.
<i>Power-On Self-Test routines (POST)</i>	Basic details.	Error Messages, EMU and suggestions for corrective action.	New features.			Error codes and suggestions for corrective action. Order of tests.
<i>Kayak diagnostic utility</i>	HP DiagTools, CD-ROM recovery.	HP DiagTools, CD-ROM recovery	New features			Technical details.
<b>Peripheral Devices</b>						
<i>Audio Accessories</i>	Refer to Audio User's Guide for information on setting up and configuring audio accessories.	Refer to online version of Audio User's Guide for information on setting up and configuring audio accessories.				



	<b>User's Guide</b>	<b>Troubleshooting Guide<sup>1</sup></b>	<b>Training Module</b>	<b>Service Handbook</b>	<b>Technical Information</b>	<b>Technical Reference Manual</b>
<i>LAN Accessories</i>	Refer to LAN Administrator's Guide for information on setting up and configuring LAN cards and systems.	Refer to online version (preloaded on hard disk) of LAN Administrator's Guide for information on setting up and configuring LAN cards and systems.				

<sup>1</sup>. For address, ["Access HP World Wide Web Site" on page 22.](#)

## 1 System Overview

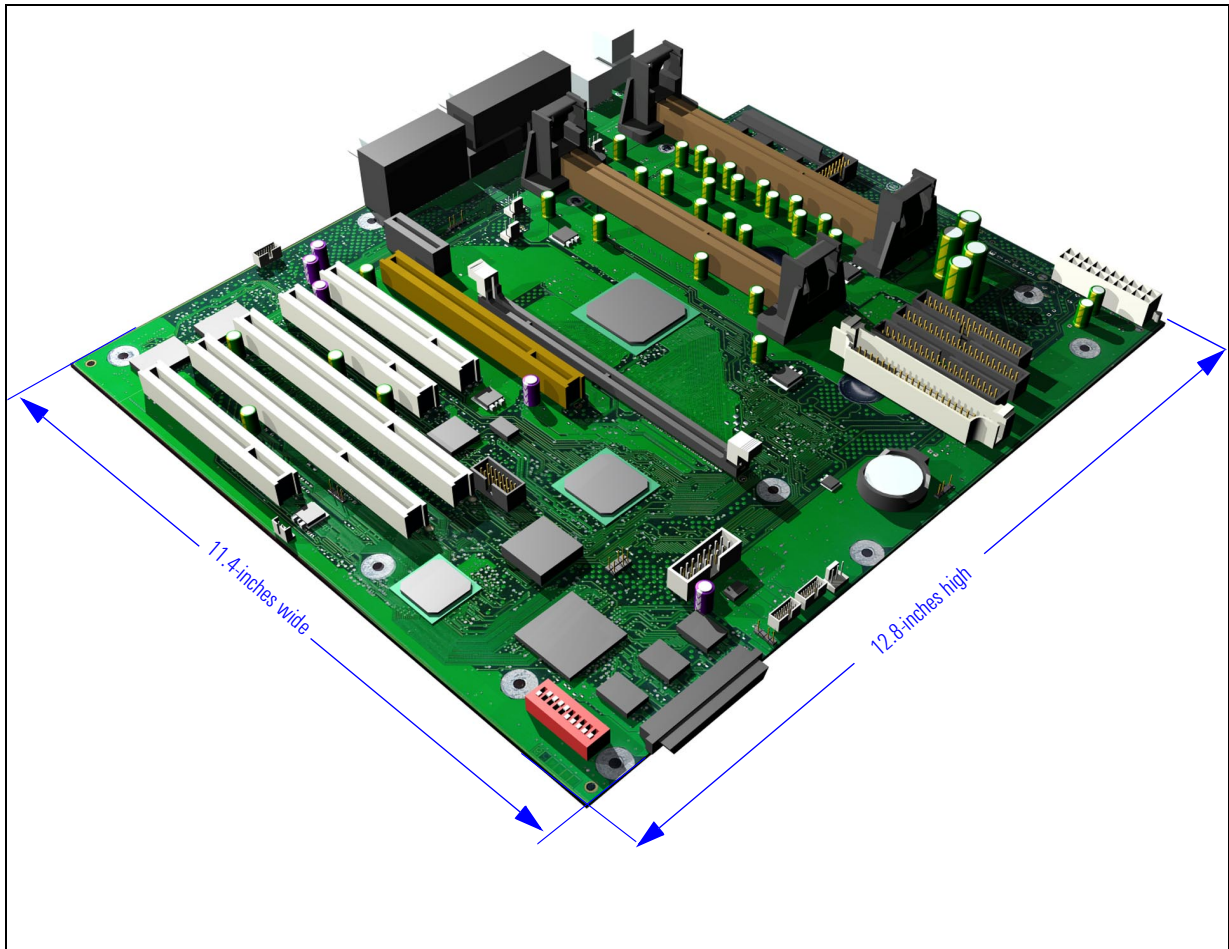
Documentation

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## System Board

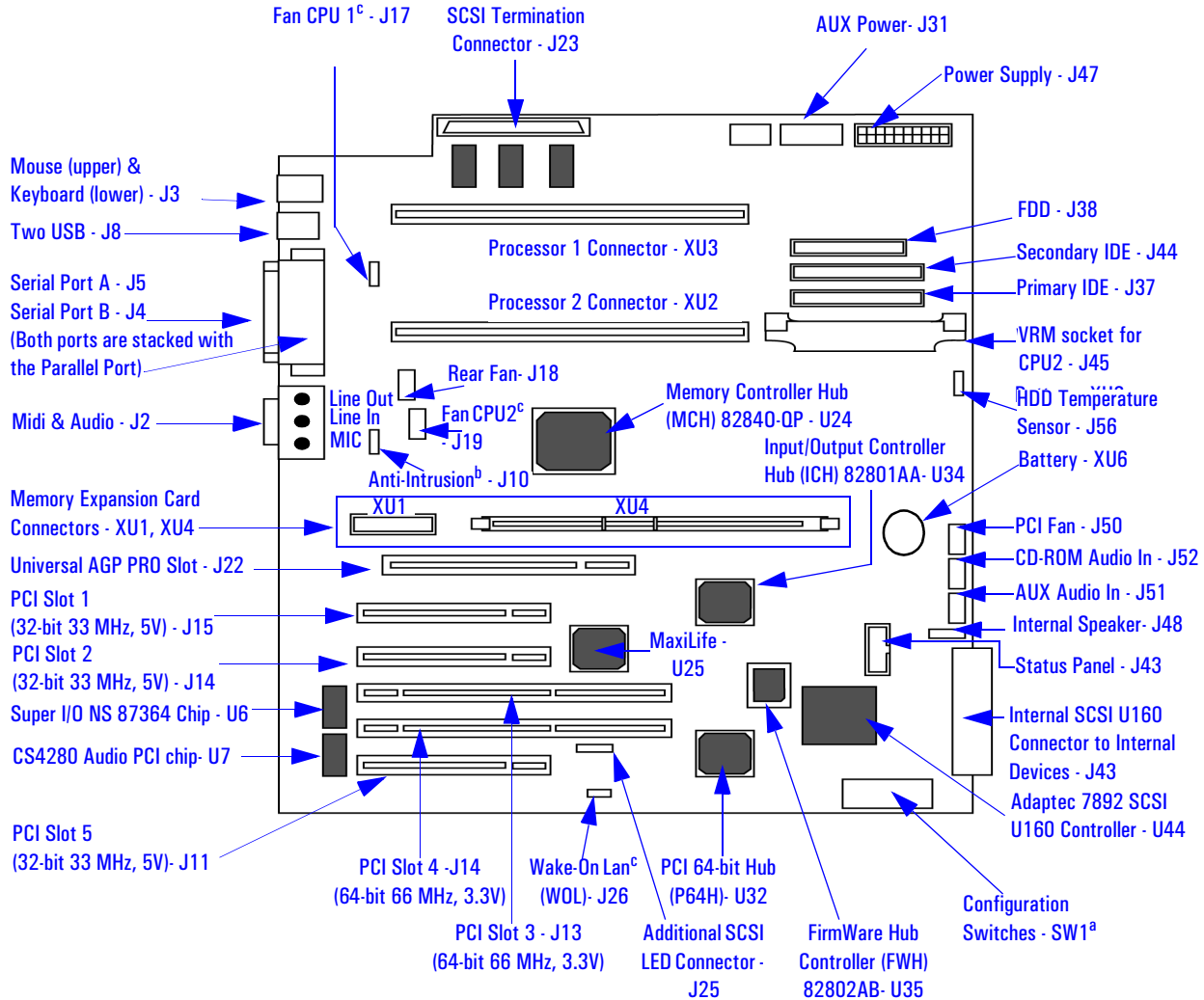
This chapter describes the components of the system board, taking in turn the components of the Memory Controller Hub (MCH), the Input/Output Controller Hub (ICH), FirmWare Hub (FWH) and the Host Bus.

The following diagram shows in detail the *HP Kayak XU800 PC Workstation* Extended ATX (E-ATX) system board.



## System Board Overview

The following diagram shows where the different chips and connectors are located on the E-ATX system board.



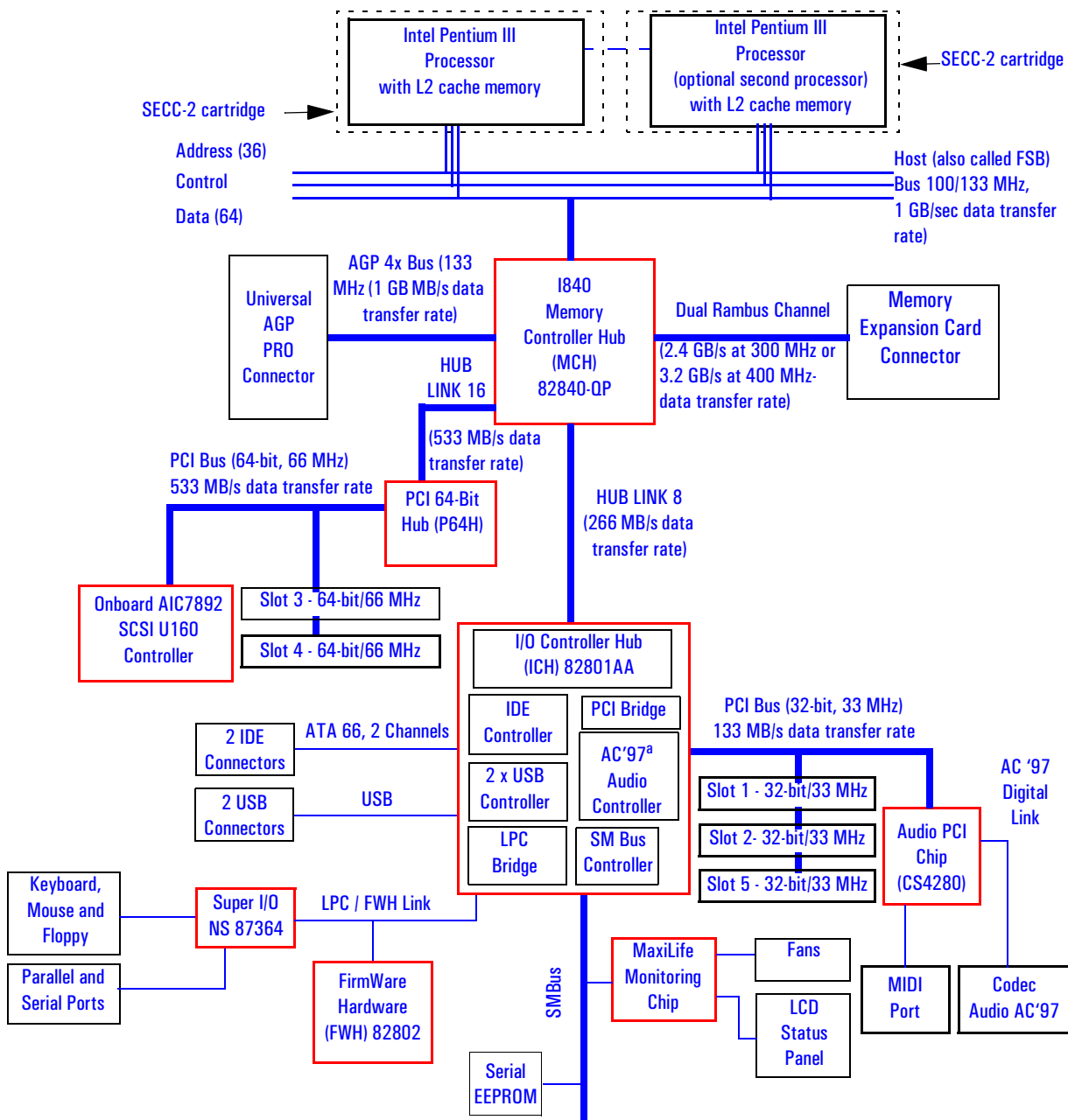
a. Refer to ["Switch Boxes" on page 33](#) or the Switch Block Label located on the chassis of the system box for the different system board switch settings.

b. Connector for the Anti-Intrusion switch.

c. Optional.

d. Connector for additional control of HDD LED on the status panel through the SCSI controller on a PCI add-on card.

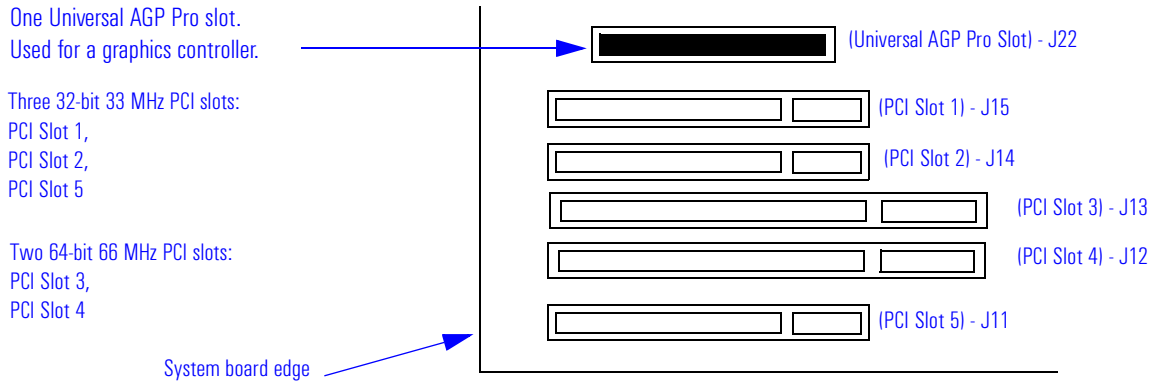
## Architectural View



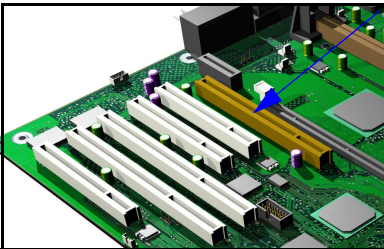
a. It should be noted that the AC'97 Audio Controller is not used. The PCI CS4280 and CS4297 audio is a full PCI solution that is independent of the ICH core logic.

## Accessory Card Slots

The following block diagram shows the position of the accessory card slots on the system board.



### Universal AGP Pro Slot



The Universal AGP Pro (Accelerated Graphics Port) bus, provides a high-performance graphics interface. It uses a 66.6 MHz base clock, and provides a peak bandwidth of 1064 MB/second in AGP 4x mode.

The Universal AGP Pro slot is a Universal-type connector which provides power through 3.3 V, 12 V or 5 V power rails with a maximum allocated power consumption of 50 W.

The Universal AGP Pro slot supports AGP 1x and 2x modes (uses 3.3 V or 1.5 V signals), and AGP 4x mode (1.5 V signalling is required).

Supported operation in the Universal AGP Pro Slot	AGP Video Card <sup>1</sup>					
	1.5 V		Universal		3.3 V	
	≤ 25 W	≤ 50 W	≤ 25 W	≤ 50 W	≤ 25 W	≤ 50 W
AGP1x <sup>2</sup>	yes	yes	yes	yes	yes	yes
AGP2x <sup>2</sup>	yes	yes	yes	yes	yes	yes
AGP4x <sup>2</sup>	yes	yes	yes	yes	no	no
PCI-type	yes	yes	yes	yes	yes	yes

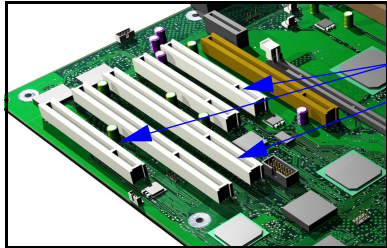
- AGP Pro video cards are supported up to 50 W.
- With or without sideband addressing.

AGP 4x mode transfers data at twice the speed of AGP 2x mode, which is itself twice the speed of the basic AGP 1x mode. This is achieved by multiplying the 66 MHz AGP clock frequency, so that four packets of data are transferred on each cycle (transfers on both rising and falling edges of the clock speed). Each packet of data contains four bytes, giving a transfer rate of 66.6 MHz x 4 (quad-clock mechanism) x 4 bytes, a maximum bandwidth of 1064 MB/s.

The AGP interface and bus are explained on [page 38](#).

### PCI Slots

There is a total of five Peripheral Component Interconnect (PCI) connectors on the system board:



- Three 32-bit 33 MHz PCI slots: 1, 2 and 5.
- Two 64-bit 66 MHz PCI slots: 3 and 4.

The three 32-bit/33 MHz PCI slots accept 5 V PCI cards and Universal PCI cards (support for 3.3 V or 5 V), while the two 64-bit/66 MHz PCI slots support 3.3 V PCI cards and Universal PCI cards (support for 3.3 V or 5 V).

A universal compatible 32-bit 33 MHz accessory card can also be installed in PCI slots 3 or 4. However in this case the PCI 64-bit bus will only perform at 33 MHz.

The maximum supported power consumption per slot is 25W, from the 5V and/or the 3.3V supply, and must respect the electrical specifications of the PCI 2.2 specification. The power consumption of each PCI board is automatically reported to the system through the two Presence Detect pins of each PCI slot. These pins code the following cases:

- No accessory board in the PCI slot.
- 7 W maximum PCI board in the PCI slot.
- 15 W maximum PCI board in the PCI slot.
- 25 W maximum PCI board in the PCI slot.

If a standard AGP (Accelerated Graphics Port) card is installed in the AGP Pro slot, the maximum power consumption for the PCI accessory and AGP slot must not exceed 100 W.

## 2 System Board

### Accessory Card Slots

If an AGP Pro card (>25 W and ≤50 W) is installed, then the PCI slot 1 is made inaccessible as defined in the AGP Pro specification (PCI slot must be left unoccupied to provide its sources, in terms of cooling and electrical power, to the AGP Pro card. The following table shows the various PCI board installations for the different PCI slots:

PCI Card										
	5 V		3.3 V				Universal (3.3 V or 5 V compatible)			
PCI Slot	32-bit/ 33 MHz	64-bit/ 33 MHz	32-bit/ 33 MHz or 66 MHz		64-bit/ 33 MHz or 66 MHz		32-bit/ 33 MHz or 66 MHz		64-bit/ 33 MHz or 66 MHz	
Slots 1, 2 & 5 5 V, 32-bit/33 MHz	yes	yes <sup>1</sup>	not supported		not supported		yes	yes <sup>2</sup>	yes <sup>1</sup>	yes <sup>1,2</sup>
Slots 3 and 4 3.3 V, 64-bit/66 MHz	not supported	not supported	33 MHz	66MHz	33 MHz	66 MHz	33 MHz	66 MHz	33 MHz	66 MHz
			yes <sup>3,4</sup>	yes <sup>4</sup>	yes <sup>3</sup>	yes	yes <sup>3,4</sup>	yes <sup>4</sup>	yes <sup>3</sup>	yes

1. A 64-bit card can be installed in a 32-bit slot. However, this card will only operate in 32-bit mode.
2. A 66 Mhz card can be installed in a 33 MHz slot. However, this card will only operate in 33 MHz mode.
3. A 33 MHz card can be installed in a 66 MHz slot, However, the card will operate in 33 MHz mode and will force all other PCI devices to operate at 33 MHz as well.
4. A 32-bit card can be installed in a 64-bit slot without preventing other 64-bit PCI devices to operate in 64-bit mode.

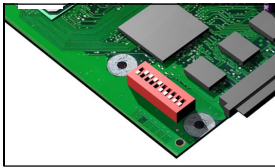
The system board and BIOS support the PCI specification 2.2. This specification supports PCI-to-PCI bridges and multi-function PCI devices, and each of the five PCI slots have Master capabilities.

PCI slots 1, 2 and 5 are connected to the ICH PCI 32-bit 33 MHz bus, while PCI slots 3 and 4 are connected to the PCI 64-bit 66 MHz bus via the P64H. In addition to these PCI slots, the following devices are also connected to a PCI Bus:

PCI 32-bit/33 MHz Bus	PCI 64-bit/66 MHz Bus
ICH (Input/Output Controller Hub) chip, bridge between the MCH (Memory Controller Hub), USB ports and IDE buses.	
Digital audio CS4280 controller.	
	Onboard AIC7892 SCSI U160 controller.

The PCI 64-bit 66 MHz bus is explained on [page 45](#). The PCI 32-bit 33 MHz bus is explained on [page 53](#).





## System Board Switches

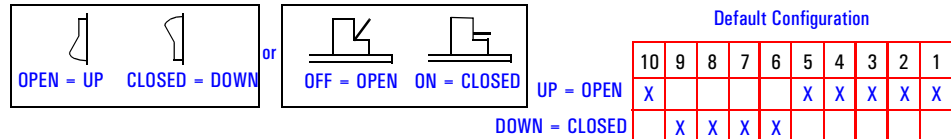
There are ten system board switches used for configuration, numbered from 1 to 10. Of these a certain number are reserved and should not be modified, otherwise it could lead to a system failure.

Switch	Default Position	Function:
1	UP	UP enables normal mode.
		DOWN enables the BIOS recovery mode at next boot.
2	UP <sup>1</sup>	UP allows Processor(s) to automatically choose the FSB speed.
		DOWN forces the FSB speed to 100 MHz.
3	UP	UP enables User and System Administrator passwords.
		DOWN clears the passwords at next boot.
4	UP	UP retains CMOS memory.
		DOWN clears CMOS memory at next boot.
5	UP <sup>1</sup>	UP = Automatic FSB frequency setting.
		DOWN = Sets operation to 133 FSB/300 Rambus.
6	DOWN <sup>1</sup>	UP. AGP™ 110 W cards appear as 50 W.
		DOWN enables AGP 110 W detection.
7	DOWN <sup>1</sup>	UP disables keyboard power-on.
		DOWN enables keyboard power-on.
8	DOWN <sup>1</sup>	UP forces the PCI 64 bus to 33 MHz if slots 3 and 4 are empty.
		DOWN disables this option.
9	DOWN <sup>1</sup>	UP disables this option.
		DOWN enables spread spectrum clocking.
10	UP <sup>1</sup>	UP Disables this option.
		DOWN provides 3.3 V Stdby to AGP Pro connector.

<sup>1</sup>. These are default settings and should not be changed.

## Switch Boxes

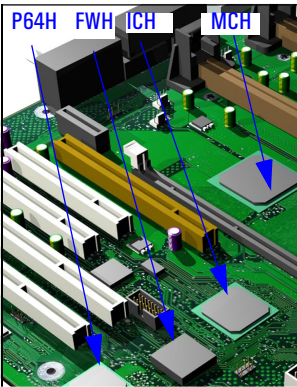
There are two types of system board switch boxes that may be used on the *HP Kayak XU800 PC Workstation*.



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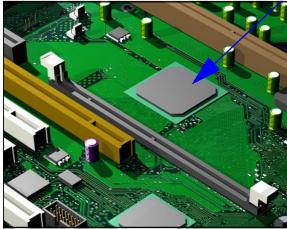
## Chipset

The Intel® I840 chipset is a high-integration chipset designed for graphics/multimedia PC platforms and is comprised of the following:



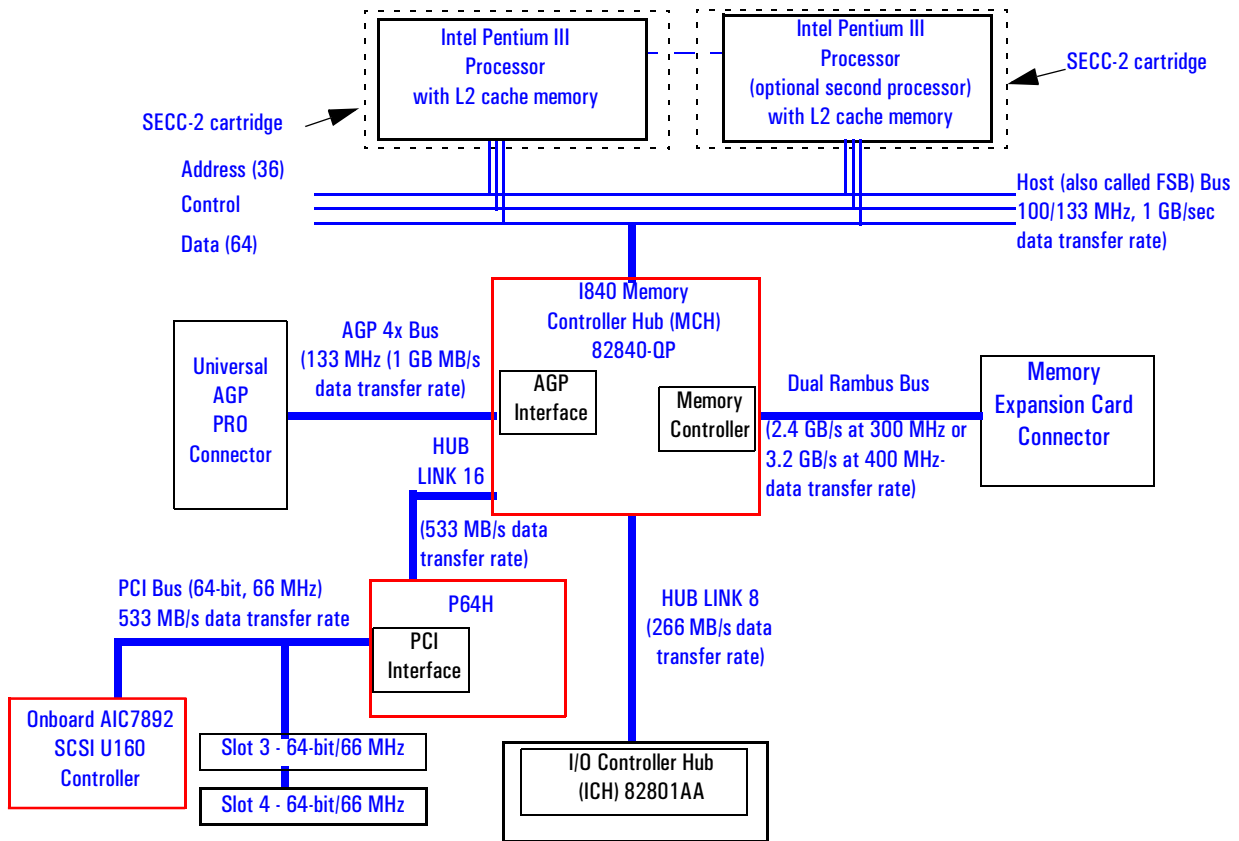
- The 82840 Memory Controller Hub (MCH) is a bridge between: the Host bus, Dual Rambus bus (main memory), the PCI bus (64-bits/66 MHz), AGP 4x (graphic) bus, Hub Link 8-bit and Hub Link 16-bit, and the PCI 64-bit Hub (P64H). The MCH chip feature is described in detail on [page 35](#).
- The PCI 64-bit Hub (P64H) performs PCI bridging between the MCH and the PCI 64-bit 66 MHz bus. The P64H is described in detail on [page 44](#).
- The 82801AA Input/Output Controller Hub (ICH) is a bridge between the following buses: the PCI bus (32-bits/33 MHz) and SMBus. In addition, the ICH supports the integrated *IDE controller (Ultra ATA/66)*, *Enhanced DMA controller*, *USB controller*, *Interrupt controller*, *Low Pin Count (LPC) interface*, *FWH interface*, *ACPI Power Management Logic*, *AC'97 2.1 Compliant Link*, *AOL (Alert-On-LAN)* and *Real Time Clock (RTC)* and *CMOS*. The ICH is described in detail on [page 48](#).
- The 82802AB Firmware Hub (FWH) stores system BIOS and SCSI BIOS, nonvolatile memory component. In addition, the FWH contains an Intel® Random Number Generator (RNG). The RNG provides random numbers to enable fundamental security building blocks for stronger encryption, digital signing and security protocols for the PC Workstation. The FWH is described in detail on [page 62](#).

## Memory Controller Hub (8240)



The MCH Host Bridge/Controller is contained in a 544-pin Ball Grid Array (BGA) package and is the bridge between the Host bus, Dual Rambus bus (main memory), AGP 4x (graphic) bus, Hub Link 8-bit and Hub Link 16-bit.

The following figure shows an example of the system block diagram using the MCH.



## 2 System Board

### Memory Controller Hub (8240)

The following table shows the features that are available in the MCH Host Bridge/Controller.

Feature	Feature
<ul style="list-style-type: none"> <li>• Processor/Host Bus:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Supports up to two Pentium III processors at: 100 MHz/133 MHz Host Bus frequency.</li> <li><input type="checkbox"/> Supports full Symmetric Multiprocessor (SMP) Protocol for up to two processors.</li> <li><input type="checkbox"/> Provides an 8-deep In-Order Queue supporting up to eight outstanding transaction requests on the host bus.</li> <li><input type="checkbox"/> Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power).</li> <li><input type="checkbox"/> Support for 36-bit host bus address.</li> <li><input type="checkbox"/> IERR and BERR signals generate SCI/SERR.</li> <li><input type="checkbox"/> Parity protection on address and resource signals: Parity errors generate SERR.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• Accelerated Graphics Port (AGP) Interface:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Single Universal AGP PRO connector.</li> <li><input type="checkbox"/> AGP Rev 2.0 compliant, including AGP 4x data transfers and 2x/4x Fast Write protocol.</li> <li><input type="checkbox"/> AGP Universal Connector support via dual mode buffers to allow AGP 2.0 3.3 V or 1.5 V signalling.</li> <li><input type="checkbox"/> AGP PIPE# or SBA initiated accesses to DRAM is not snooped</li> <li><input type="checkbox"/> AGP FRAME initiated accesses to DRAM are snooped (snooper identifies that data is coherent in cache memory).</li> <li><input type="checkbox"/> Hierarchical PCI configuration mechanism.</li> <li><input type="checkbox"/> Delayed transaction support for AGP-to-DRAM reads that cannot be serviced immediately.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>• Memory Controller.</li> </ul> <p><b>Direct Rambus:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Dual Direct Rambus Channels operating in lock-step (both channels must be populated with a memory module). Supporting 300 MHz or 400 MHz.</li> <li><input type="checkbox"/> RDRAM 64 Mb, 128 Mb, 256 Mb devices.</li> <li><input type="checkbox"/> Minimum upgrade increment of 16 MB using 64 Mb DRAM technology.</li> <li><input type="checkbox"/> Up to 64 Direct Rambus devices (without using MRH-R). Dual channel maximum memory array size is:           <ul style="list-style-type: none"> <li>– 512 MB using 64 Mb DRAM technology.</li> <li>– 1 GB using 128 Mb DRAM technology.</li> <li>– 2 GB using 256 Mb DRAM technology.</li> </ul> </li> <li><input type="checkbox"/> Up to 8 simultaneous open pages:           <ul style="list-style-type: none"> <li>– 1 KByte page size support for 64 Mbit, 128 Mbit and 256 Mbit RDRAM devices.</li> <li>– KByte page size support for 256 Mbit RDRAM devices.</li> </ul> </li> </ul>	<p><b>SDRAM:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Up to 8 GB of SDRAM using four external Memory Repeater Hubs for SDRAM (MRH-S). <u>Currently, two MRH-S devices are supported.</u></li> <li><input type="checkbox"/> Interleaved 100 MHz support using 4 MRH-S for a maximum bandwidth.</li> <li><input type="checkbox"/> Non-Interleaved 100 MHz support using 2 MRH-s for lower cost and upgrade path.</li> <li><input type="checkbox"/> Unbuffered DIMMs are supported.</li> <li><input type="checkbox"/> Up to 4 rows or 2 DS DIMMs per MRH-S.</li> <li><input type="checkbox"/> Up to 8 simultaneous open pages:           <ul style="list-style-type: none"> <li>– 2 KByte page size support for 64 Mbit SDRAM devices.</li> <li>– 4 KByte - 16 KByte page sizes supporting 64 MBit to 256 Mbit SDRAM devices.</li> </ul> </li> <li><input type="checkbox"/> Configurable optional ECC operation:           <ul style="list-style-type: none"> <li>– ECC with single bit Error Correction and multiple bit Error Detection.</li> <li>– Single bit errors corrected and written back to memory (scrubbing).</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>• Hub Link 8-bit Interface to ICH:               <ul style="list-style-type: none"> <li><input type="checkbox"/> High-speed interconnect between the MCH and ICH (266 MB/sec).</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• Hub Link 16-bit Interface to P64H:               <ul style="list-style-type: none"> <li><input type="checkbox"/> High-speed interconnect between the MCH and P64H (533 MB/sec).</li> </ul> </li> </ul>

Feature	Feature
<ul style="list-style-type: none"> <li>• Power management:               <ul style="list-style-type: none"> <li><input type="checkbox"/> SMRAM space re-mapping to A0000h - BFFFFh (128 KB).</li> <li><input type="checkbox"/> Extended SMRAM space above 256 MB, additional 128 K, 256 K, 512 K, 1 MB TSEG from Top of Memory, cacheable (cacheability controlled by processor).</li> <li><input type="checkbox"/> Suspend to RAM.</li> <li><input type="checkbox"/> ACPI Rev. 1.0 compliant power management.</li> <li><input type="checkbox"/> APM Rev. 1.2 compliant power management.</li> <li><input type="checkbox"/> Power-managed states are supported for up to two processors.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• Arbitration:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Distributed Arbitration Model for Optimum Concurrency Support.</li> <li><input type="checkbox"/> Concurrent operations of host, hub interface, AGP and memory buses supported via a dedicated arbitration and data buffering logic.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>• 544 mBGA MCH package.</li> </ul>	<ul style="list-style-type: none"> <li>• Input/Output Device Support:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Input/Output Controller Hub (ICH).</li> <li><input type="checkbox"/> PCI 64 Hub (P64H).</li> </ul> </li> </ul>

## MCH Interface

The MCH interface provides bus control signals and address paths via the Hub Link 8-bit access to the ICH and via the Hub Link 16-bit access to the P64H for transfers between the processor(s) on the Host bus (FSB), Dual Rambus bus and AGP 4x bus.

The MCH supports 36-bit host addresses, allowing the processor to address a space of 64 GB. It also provides an 8-deep In-Order Queue supporting up to eight outstanding transaction requests on the host bus.

Host-initiated input/output signals are positively decoded to AGP, Hub Link 16-bit interface, or MCH configuration space and subtractively decoded to Hub Link 8-bit interface. Host-initiated memory cycles are positively decoded to AGP, Hub Link 16-bit interface, or DRAM, and are again subtractively decoded to Hub Link 8-bit interface.

AGP semantic memory accesses initiated from AGP to DRAM do not require a snoop cycle (not snooped) on the Host bus, since the coherency of data for that particular memory range will be maintained by the software. However, memory accesses initiated from AGP using PCI Semantics and accesses from either Hub Link interface (8-bit or 16-bit) to DRAM do require a snoop cycle on the Host bus.

Memory access whose addresses are within the AGP aperture are translated using the AGP address translation table, regardless of the originating interface.

## 2 System Board

### Memory Controller Hub (8240)

Write accesses from Hub Link interface (8-bit or 16-bit) to the AGP are supported.

The MCH can support one or two Pentium III processors, at FSB frequencies of 100/133 MHz using GTL+ signalling. Refer to [page 64](#) for a description of the Host bus.

### Accelerated Graphics Port (AGP) Bus Interface

A controller for the Universal AGP (Accelerated Graphics Port) Pro slot is integrated in the MCH. The AGP Bus interface is compatible with the Accelerated Graphics Port Specification, Rev 2.0, operating at 133 MHz, and supporting up to 1 GB/sec data transfer rates. The MCH supports only a synchronous AGP interface, coupling to the Host bus frequency.

### AGP 4x Bus

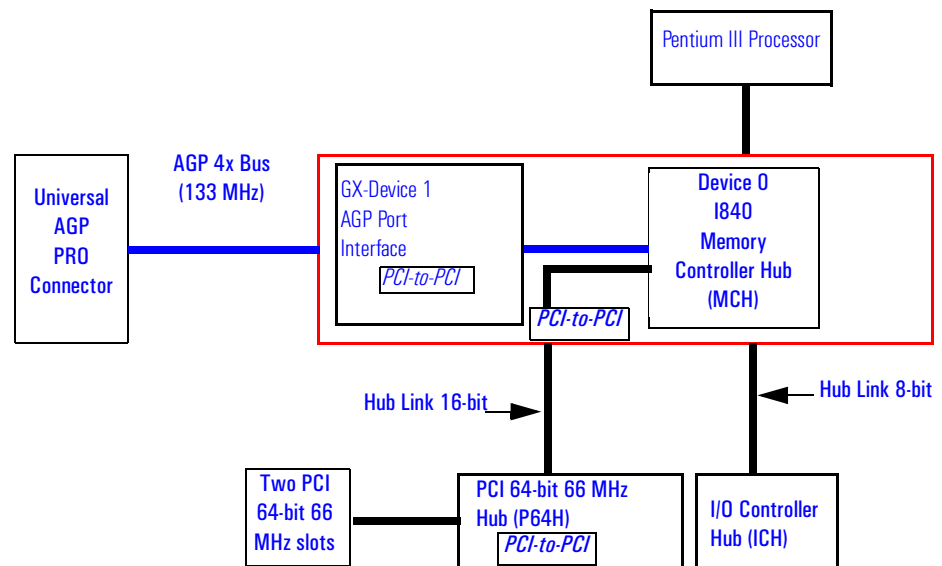
The AGP bus is a dedicated bus for the graphics subsystem, which meets the needs of high quality 3D graphics applications. It has a direct link to the MCH

The AGP bus is based upon a 66 MHz, 32-bit PCI bus architecture, to which several signal groups have been added to provide AGP-specific control and transfer mechanisms.

AGP specific transactions always use pipelining. This control mechanism increases the bus efficiency for data transfer. Sideband Addressing (SBA) may also be used by AGP transaction requests which further increases the bus efficiency for data transfer. The supported modes are detailed below:

- FRAME based AGP. Only the PCI semantics are: 66 MHz, 32-bit, 3.3 V, 266 MB/s peak transfer rate.
- AGP 1X with pipelining, sideband addressing can be added: uses 66 MHz, 32-bit, 3.3 V, increased bus efficiency, 266 MB/s peak transfer rate.
- AGP 2X with pipelining, sideband addressing can be added: 66 MHz double clocked, 32-bit, 3.3 V, 533 MB/s peak transfer rate.
- AGP 4X with pipelining, sideband addressing can be added: 133 MHz double clocked, 32-bit, 1.5 V, increased bus efficiency, 1066 MB/s peak transfer rate

## AGP PCI Bus Implementation



### Main Memory Controller

The main memory controller is integrated in the MCH supporting two primary rambus channels (A and B).

### DRAM Interface

The MCH provides optional Host bus error checking for data, address, request and response signals. Only 300 MHz and 400 MHz Direct Rambus devices are supported in any of 64, 128 or 256 Mb technology. 64 and 128 MBit RDRAMs use page sizes of 1 kbytes, while 256 Mb devices target 1 kbyte or 2 kbyte pages.

A maximum number of 64 Rambus devices (32 devices maximum per channel) is supported. Both channels must be populated with *paired* memory modules.

## 2 System Board

### Memory Controller Hub (8240)

The following table shows the number of Rambus devices and memory technology available on a memory module.

Number of devices per RIMM	Memory Technology (number of Megabits)		
	64 Mbits	128 Mbits	256 Mbits
4	N/A	64 MB module	128 MB module
8	N/A	128 MB module	256 MB module
16	128 MB module	256 MB module	512 MB module

MCH also provides optional data integrity features including ECC in the memory array. During DRAM writes, ECC is generated on a QWord (64 bit) basis. During DRAM reads, the MCH supports multiple-bit error detection and single-bit error correction when the ECC mode is enabled.

MCH will scrub single bit errors by writing the corrected value back into DRAM for all reads when hardware scrubbing is enabled. This, however does not include reads launched in order to satisfy an AGP transaction.

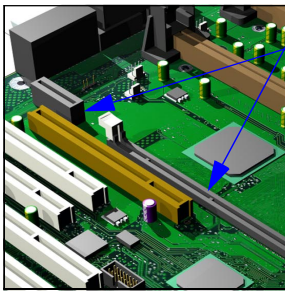
### Dual Rambus Bus

The Dual Rambus bus is comprised of 16 x 2 bits of data information, and 8 bits of Error Correcting Code (ECC). The bus is connected to the Memory Expansion Card Connector and to the MCH chip supporting two Dual Rambus channels (A and B).

Both channels run at 300 or 400 MHz supporting up to 32 rambus devices per channel (individual chips) or one MRH-S (Memory Repeater Hub) per channel for DIMM sockets. The maximum available data bandwidth is 3.2 GB/s at 400 MHz.

The configuration of both primary rambus channels must be symmetrical. That is to say, whatever the configuration on channel A, the same must be on channel B.





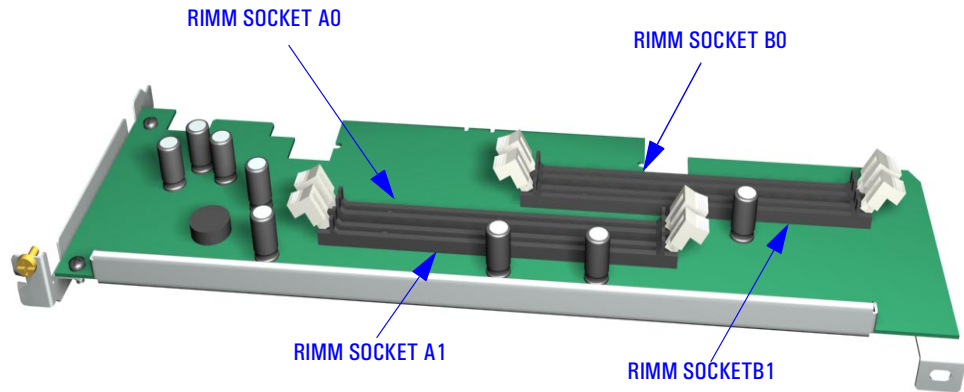
### Memory Expansion Card Connector

The actual memory array is on a Memory Expansion Card installed in a Memory Expansion Card Connector (MECC) located on the system board.

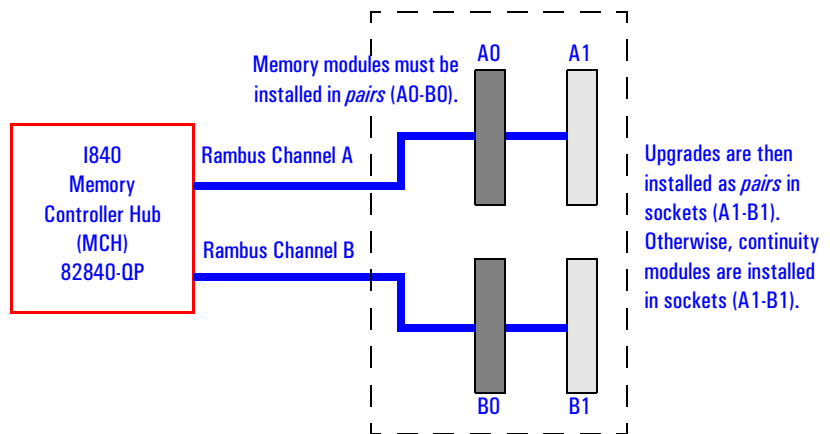
On the *HP Kayak XU800 PC Workstation* there are two types of Memory Expansion Cards supporting the following configurations:

### Four-RIMM Memory Expansion Card

Four RIMM sockets support RDRAM ECC and memory modules installed in *pairs*. Any unused RIMM sockets must contain a continuity module.



Models are supplied with either 128 MB or 256 MB RDRAM ECC main memory. Memory upgrades are available in *pairs* of RIMMs, with an individual RIMM size of 64 MB, 128 MB, 256 MB or 512 MB. The following diagram shows installed memory. There are always two RIMMs working in parallel.



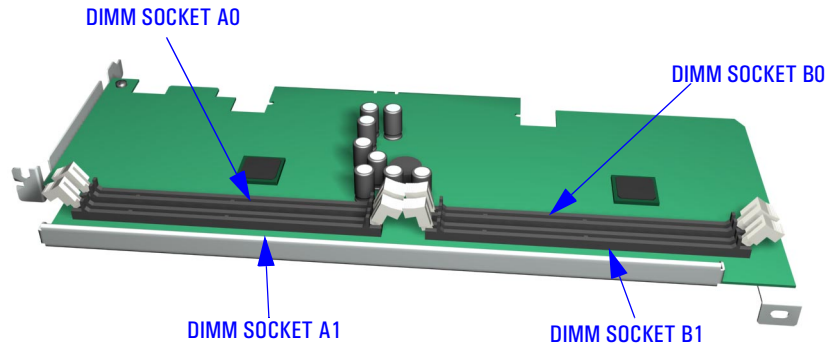
Each RIMM socket is connected to the SMBus and is described on [page 57](#).

## 2 System Board

Memory Controller Hub (8240)

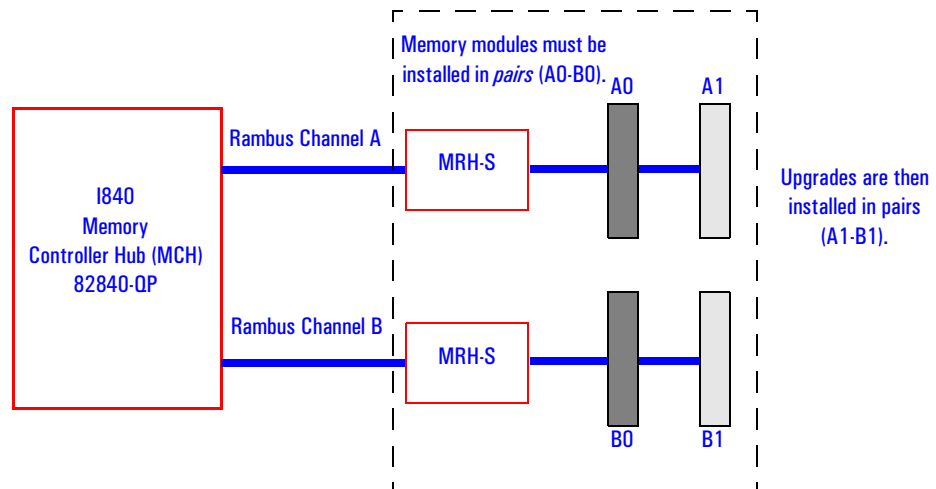
### Four-DIMM Memory Expansion Card

Four DIMM sockets support SDRAM 100 MHz unbuffered ECC memory modules installed in *pairs*. Unused DIMM sockets can be left free.



The MCH supports one Rambus Memory Hub for SDRAM (MRH-S) per connected channel. Each MRH-S allows bridging of a single SDRAM channel on to the main Rambus channel. The MRH-S also translates RDRAM and SDRAM protocols, thus enabling the DIMM Memory Expansion Card to be used on the Rambus channels.

As only one MRH-S is connected to each channel, the MCH operates the MRH-S pair in non-interleaved mode.



Models are supplied with 128 MB of SDRAM unbuffered ECC main memory. Memory upgrades are available in 64 MB, 128 MB, 256 MB or 512 MB unbuffered 100 MHz ECC SDRAM modules.

MRH-S (Memory Repeater Hub-SDRAM) provides support for two double-sided 100 MHz SDRAM DIMM sockets.

Each DIMM socket is connected to the SMBus and is described on [page 57](#).

### Read/Write Buffers

The MCH defines a data buffering scheme to support the required level of concurrent operations and provide adequate sustained bandwidth between the DRAM subsystem and all other system interfaces (CPU, AGP and PCI).

### System Clocking

The MCH operates the host interface at 100 MHz or 133 MHz, PCI at 33 MHz and AGP at 66/133 MHz. Coupling between all interfaces and internal logic is done in a synchronous manner. The clocking scheme uses an external clock synthesizer (which produces reference clocks for the host, AGP and PCI interfaces).

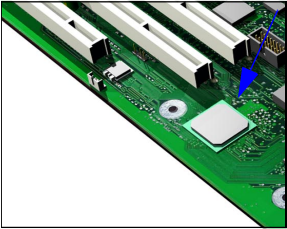
### I/O APIC

I/O APIC is used to support dual processors as well as enhanced interrupt processing in the single processor environment. The I/O APIC controller of the ICH is used in conjunction with a second I/O APIC controller in the P64H.

## 2 System Board

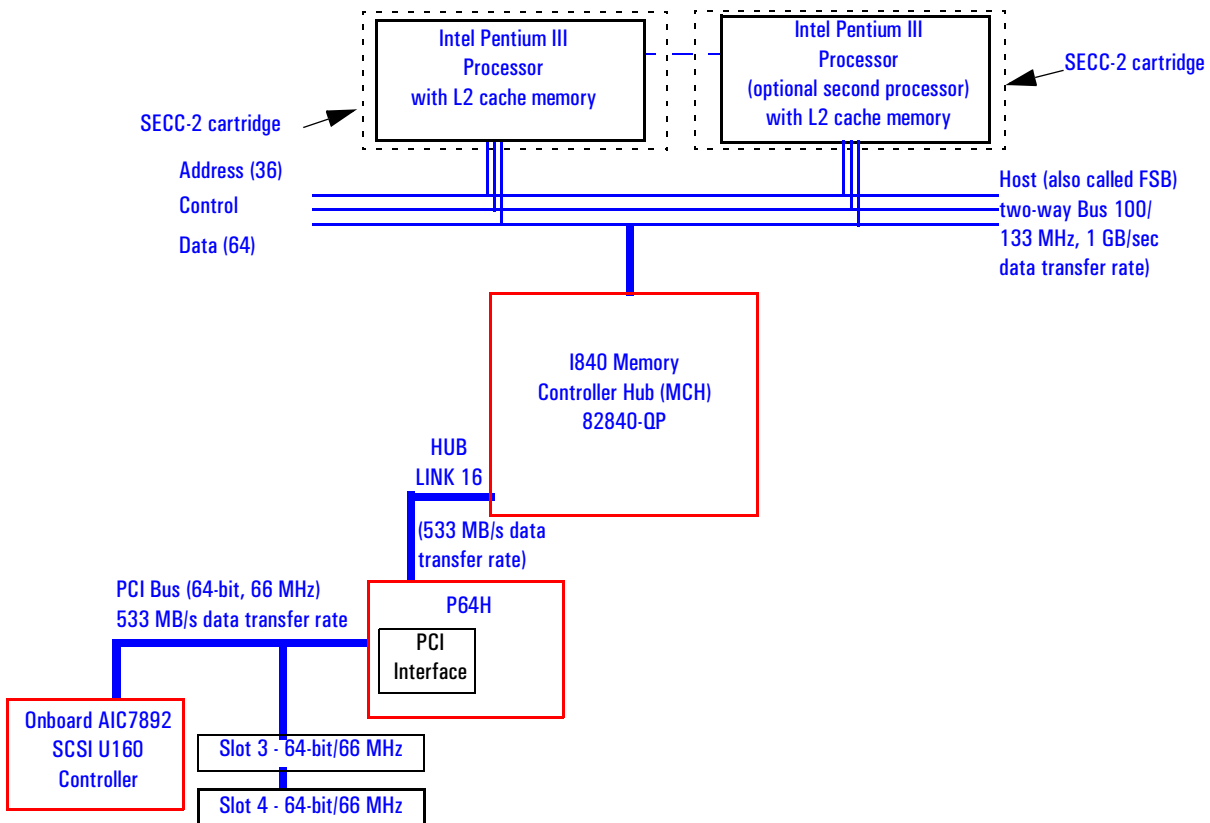
### PCI 64-bit Hub

## PCI 64-bit Hub



The P64H is a peripheral chip that performs PCI bridging functions between the MCH and the PCI 64-bit 66 MHz bus. The P64H has a 16-bit primary hub interface to the MCH and a secondary 64-bit PCI bus interface. This controller inter-operates transparently with either 64-bit or 32-bit devices.

The following figure shows how the P64H chip is connected to the MCH via the Hub Link 16 and to the supported devices such as those in the two PCI 64-bit 66 MHz PCI slots and AIC-7892 Ultra 160 SCSI controller via the PCI 64-bit 66 MHz bus.



The following table shows the available P64H features.

Feature	Feature
<ul style="list-style-type: none"> <li>• PCI Interface:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Both 64-bit and 32-bit 33 MHz or 66 MHz devices.</li> <li><input type="checkbox"/> Provides Synchronous operation to the P64H using 1:1(66 MHz) or 2:1 (33 MHz) hub interface/PCI bus gearing ratio.</li> <li><input type="checkbox"/> Allows input/output operations to occur with processor transactions to isolate traffic.</li> <li><input type="checkbox"/> Parity and System Error (PERR# / PERR#).</li> <li><input type="checkbox"/> Allows peer-to-peer communication within a single PCI bus segment.</li> <li><input type="checkbox"/> Provides PCI transaction forwarding for all I/O and memory (Type 1-to-Type 1, Type 1-to-Type 0, Type 1 to a special cycle).</li> <li><input type="checkbox"/> Provides address decoding for:                   <ul style="list-style-type: none"> <li>16-bit I/O addressing.</li> <li>32-bit memory mapped I/O addressing.</li> <li>44-bit prefetchable memory addressing (upstream only).</li> <li>VGA addressing.</li> </ul> </li> <li><input type="checkbox"/> Includes downstream LOCK# capabilities.</li> <li><input type="checkbox"/> Fast Back-to-Back cycles (upstream only).</li> <li><input type="checkbox"/> Bus parking.</li> <li><input type="checkbox"/> Implements Delayed Transaction for;                   <ul style="list-style-type: none"> <li>PCI configuration read/written I/O read, and memory read commands (downstream).</li> <li>Memory read, I/O read and I/O write commands (upstream).</li> </ul> </li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• Scalability / Flexibility:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Provides arbitration support for all PCI devices.</li> <li><input type="checkbox"/> Supports 2 x 66 MHz PCI slots.</li> <li><input type="checkbox"/> Processes dual address cycle (DAC) for upstream access &gt; 4 GB.</li> <li><input type="checkbox"/> Handles 3.3 V operation with 5.0 V tolerant on all input pins.</li> </ul> </li> <li>• Upstream Hub Link 16 Interface:               <ul style="list-style-type: none"> <li><input type="checkbox"/> Connects to the MCH via a 16-bit hub interface.</li> <li><input type="checkbox"/> Provides 64-bit and 32-bit addressing.</li> <li><input type="checkbox"/> Utilizes 66 MHz base clock.</li> <li><input type="checkbox"/> Utilizes 133 MHz double-clocked strobes.</li> </ul> </li> <li>• Integrated Functions:               <ul style="list-style-type: none"> <li><input type="checkbox"/> I/O APIC to provide 24 interrupts.</li> <li><input type="checkbox"/> Six copies of PCLKOUT signals to its PCI devices.</li> </ul> </li> </ul>

### PCI 64-bit 66 MHz Bus Interface

The P64H provides the interface to a PCI 64-bit 66 MHz bus interface supporting both 64-bit and 32-bit 33 MHz or 66 MHz devices.

This interface implementation is compliant with PCI Rev 2.2 Specification, and it can support up to 533 MB/sec data transfer rates.

It also supports PCI master capabilities and the Adaptec AIC 7892 16-bit Ultra 160 SCSI controller.

A table on [page 68](#) shows the P64H interrupts.

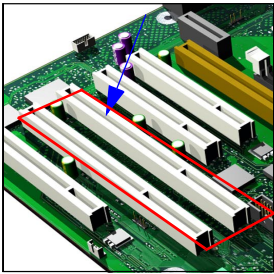
## 2 System Board

### PCI 64-bit Hub

#### Devices Supported on the PCI 64-bit 66 MHz Bus

The following devices are supported on the PCI 64-bit 66 MHz bus.

#### PCI 64-bit 66 MHz Slots



There are two PCI 64-bit 66 MHz PCI slots (slots 4 and 5) connected to the PCI 64-bit 66 MHz bus. These two 64-bit/66 MHz PCI slots support 3.3 V PCI cards and Universal PCI cards (support for 3.3 V or 5 V).

A universal compatible 32-bit 33 MHz accessory card can also be installed in PCI slots 3 or 4. However in this case the PCI 64-bit bus will only perform at 33 MHz.

PCI slots are explained in detail on [page 31](#).

#### Ultra-Wide 160 SCSI Controller

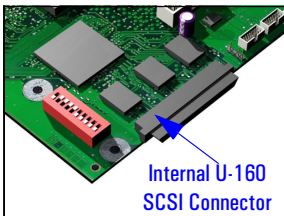
The Adaptec AIC-7892 Ultra 160 SCSI PCI controller is integrated on the system board. Data is transferred at 160 MB/s on 16-bit wide, Low Voltage Differential (LVD) bus.

---

#### NOTE

If an Ultra-wide, or older SCSI device is connected on the SCSI bus, all Ultra 160 and Ultra 2 SCSI devices will automatically be switched to Ultra-wide SCSI. In this case, the LVD bus works as a single-ended bus, and data will only be transferred at 40 MB/s.

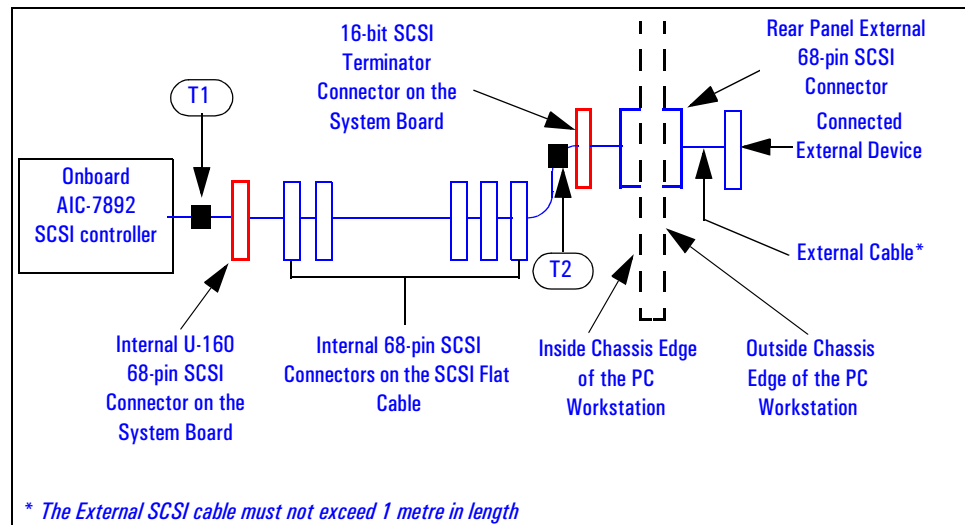
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The controller is fitted with a 16-bit SCSI flat cable with five connectors, plus a SCSI termination device on the system board; so a maximum of five internal SCSI internal devices are supported. Additional devices can be added outside the PC Workstation by connecting directly to the rear panel SCSI connector. The external connector allows up to ten external devices to be connected. This gives a maximum of 15 (internal + external) devices that can be connected.

The last connector on the SCSI cable is connected to the external SCSI connector on the rear chassis. The connector before this is connected to the onboard SCSI terminator (located behind the processor).

In the following diagram, the T1 (SCSI terminator located near the AIC-7892 SCSI controller) and T2 boxes are SCSI terminators. If an external cable is connected, then the T2 termination is automatically deactivated.



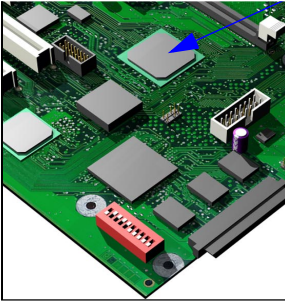
By default, the internal SCSI bus is configured to run in Ultra 160 SCSI mode (providing a maximum band-width of 160 MB/s). The user may configure the SCSI system using the *SCSISelect* utility, included in the system BIOS. Refer to [page 99](#) for details about the *SCSISelect* utility. This utility is also described in more detail in the *SCSI User's Guide*.

The Adaptec AIC-7892 Ultra 160 SCSI PCI controller is BBS compliant, but does not support Hot Swap.

## 2 System Board

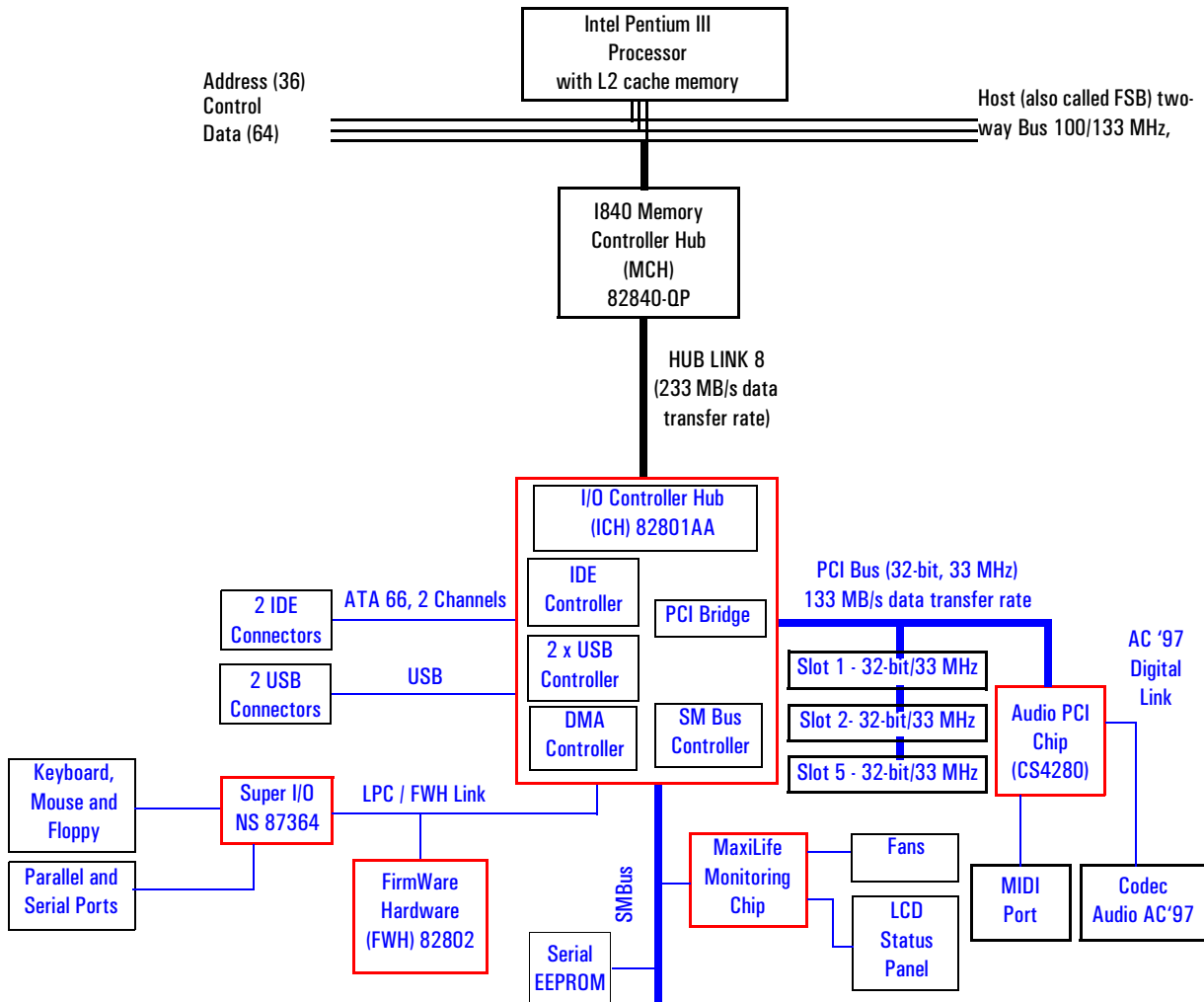
The Input/Output Controller Hub (82801AA)

### The Input/Output Controller Hub (82801AA)



The ICH, is encapsulated in a 241-pin Ball Grid Array (BGA) package and is located on the system board just underneath the Memory Expansion Card Connector. It provides the interface between the PCI bridge (PCI Rev. 2.2 compliant with support for 32-bit 33 MHz PCI operations), PCI-to-LPC (Low Pin Count) bridge, IDE controller, USB controller, SMBus controller and AC'97 controller.

The ICH functions and capabilities are discussed in detail later on in this section. The following figure shows an example of the system block diagram using the ICH.





The following table shows the available ICH features.

Feature	Feature
<ul style="list-style-type: none"> <li>● Multi-function PCI Bus Interface: <ul style="list-style-type: none"> <li><input type="checkbox"/> PCI at 32-bit 33 MHz.</li> <li><input type="checkbox"/> PCI Rev 2.2 Specification.</li> <li><input type="checkbox"/> 133 Mbyte/sec data transfer rate.</li> <li><input type="checkbox"/> Master PCI Device Support for up to six devices.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Enhanced DMA Controller: <ul style="list-style-type: none"> <li><input type="checkbox"/> Two 82C37 DMA controllers.</li> <li><input type="checkbox"/> PCI DMA with 2 PC/PCI Channels in pairs.</li> <li><input type="checkbox"/> LPC DMA.</li> <li><input type="checkbox"/> DMA Collection Buffer to provide Type-F DMA performance for all DMA channels.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● USB, supporting: <ul style="list-style-type: none"> <li><input type="checkbox"/> USB revision 1.1 compliant.</li> <li><input type="checkbox"/> UHCI Implementation with Two USB Ports for serial transfers at 12 or 1.5 Mbit/sec.</li> <li><input type="checkbox"/> Wake-up from sleeping states (refer to table on page 19).</li> <li><input type="checkbox"/> Legacy keyboard/mouse software.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Interrupt Controller: <ul style="list-style-type: none"> <li><input type="checkbox"/> Two cascaded 82C59 controllers.</li> <li><input type="checkbox"/> Integrated I/O APIC capability.</li> <li><input type="checkbox"/> 15 Interrupt support in 8259 Mode, 24 supported in I/O APIC mode.</li> <li><input type="checkbox"/> Serial Interrupt Protocol.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● Power Management Logic: <ul style="list-style-type: none"> <li><input type="checkbox"/> ACPI 1.0 compliant.</li> <li><input type="checkbox"/> Support for APM-based legacy power management for non-ACPI implementations.</li> <li><input type="checkbox"/> ACPI defined power states (S1, S3, S4, S5).</li> <li><input type="checkbox"/> ACPI power management timer.</li> <li><input type="checkbox"/> SMI generation.</li> <li><input type="checkbox"/> All registers readable/restorable for proper resume from 0 V suspend states.</li> <li><input type="checkbox"/> PCI PME#.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Integrated IDE Controller: <ul style="list-style-type: none"> <li><input type="checkbox"/> Independent Timing of up to four drives.</li> <li><input type="checkbox"/> Ultra ATA/66 Mode (66 Mbytes/sec).</li> <li><input type="checkbox"/> Ultra ATA/33 Mode (33 Mbytes/sec).</li> <li><input type="checkbox"/> PIO Mode 4 transfers up to 14 Mbytes/sec.</li> <li><input type="checkbox"/> Separate IDE connections for Primary and Secondary cables.</li> <li><input type="checkbox"/> Integrated 16 x 32-bit buffer for IDE PCI Burst transfers.</li> <li><input type="checkbox"/> Write Ping-Pong Buffer for faster write performances.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● Real-Time Clock, supporting: <ul style="list-style-type: none"> <li><input type="checkbox"/> 256-byte battery-backed CMOS RAM.</li> <li><input type="checkbox"/> Hardware implementation to indicate Century Rollover.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● System TCO Reduction Circuits: <ul style="list-style-type: none"> <li><input type="checkbox"/> Timers to Generate SMI# and Reset Upon.</li> <li><input type="checkbox"/> Timers to Detect Improper Processor Reset.</li> <li><input type="checkbox"/> Integrated Processor Frequency Strap Logic.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● Timers Based on 82C54: <ul style="list-style-type: none"> <li><input type="checkbox"/> System Timer, Refresh Request, Speaker Tone Output.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● SMBus <ul style="list-style-type: none"> <li><input type="checkbox"/> Host Interface allows processor to communicate via SMBus.</li> <li><input type="checkbox"/> Compatible with 2-wire I<sup>2</sup>C bus.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● System Timer, Refresh Request, Speaker Tone Output.</li> </ul>	<ul style="list-style-type: none"> <li>● GPIO: <ul style="list-style-type: none"> <li><input type="checkbox"/> TTL, Open-Drain, Inversion.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● Firmware Hub (FWH) interface.</li> </ul>	<ul style="list-style-type: none"> <li>● 3.3 V operation with 5 V Tolerant Buffers for IDE and PCI signals.</li> </ul>
<ul style="list-style-type: none"> <li>● 241 BGA Package.</li> </ul>	<ul style="list-style-type: none"> <li>● Alert-On-LAN (AOL) support.</li> </ul>

## 2 System Board

The Input/Output Controller Hub (82801AA)

### ICH Architecture

The ICH interface architecture ensures that the I/O subsystems, both PCI and the integrated input/output features (for example: IDE, AC'97 and USB) receive the adequate bandwidths.

To achieve this, by placing the I/O bridge directly on the ICH interface, and no longer on the PCI bus, the ICH architecture ensures that both the input/output functions integrated into the ICH and the PCI peripherals obtain the bandwidth necessary for peak performance.

### ICH PCI Bus Interface

The ICH PCI provides the interface to a PCI bus interface operating at 33 MHz. This interface implementation is compliant with PCI Rev 2.2 Specification, supporting up to six external PCI masters in addition to the ICH requests and AC'97 controller. The PCI bus can reach a data transfer rate of 133 MBytes/sec. The maximum PCI burst transfer can be between 256 bytes and 4 KB. It also supports advanced snooping for PCI master bursting, and provides a pre-fetch mechanism dedicated for IDE read.

Refer to the table [page 68](#) for ICH interrupts.

### SMBus Controller

The System Management (SM) bus is a two-wire serial bus which runs at a maximum of (100 kHz). The SMBus Host interface allows the processor to communicate with SMBus slaves and an SMBus Slave interface that allows external masters to activate power management events. The bus connects to sensor devices that monitor some of the hardware functions of the system board, both during system boot and run-time.

Refer to [page 55](#) for a description of the devices on the SMBus, or to [page 58](#) for information on the MaxiLife ASIC.

### Low Pin Count Interface

The ICH implements the LPC interface 1.0 specification.

### Enhanced USB Controller

The USB (Universal Serial Bus) controller provides enhanced support for the Universal Host Controller Interface (UHCI). This includes support that allows legacy software to use a USB-based keyboard and mouse. The USB supports two stacked connectors on the back panel. These ports are built into the ICH, as standard USB ports.

The ICH is USB revision 1.1 compliant.

USB works only if the USB interface has been enabled within the HP *Setup* program. Currently, only the Microsoft Windows 95 and Windows 98 operating systems provide support for the USB.

### AC'97 Controller

This controller, even though available in the ICH, is not used. The HP Kayak PC Workstation uses the dedicated dual chip PCI solution of the CS4280 audio controller and the CS4297 Codec Audio Codec '97 (AC'97).

Refer to [page 54](#) for information about the CS4280 and CS4297 audio solution.

### IDE Controller

The IDE controller is implemented as part of the ICH chip and has PCI-Master capability. Two independent ATA/66 IDE channels are provided with two connectors per channel. Two IDE devices (one master and one slave) can be connected per channel. In order to guarantee data transfer integrity, Ultra-ATA cables must be used for Ultra-ATA modes (Ultra-ATA/33 and Ultra-ATA/66).

The PIO IDE transfers of up to 14 Mbytes/sec and Bus Master IDE transfer rates of up to 66 Mbytes/sec are supported. The IDE controller integrates 16 x 32-bit buffers for optimal transfers.

It is possible to mix a fast and a slow device, such as a hard disk drive and a CD-ROM, on the same channel without affecting the performance of the fast device. The BIOS automatically determines the fastest configuration that each device supports.

### DMA Controller

The seven-channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit count-by-byte transfers, while channels 5 to 7 are for 16-bit count-by-word transfers (refer to table on [page 104](#) for allocated DMA channel allocations). Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

The ICH DMA controller supports the LPC (Low Pin Count) DMA. Single, Demand, Verify and Incremental modes are supported on the LPC interface. Channels 0-3 are 8-bit, while channels 5-7 are 16-bit. Channel 4 is reserved as a generic bus master request.

### Interrupt Controller

The Interrupt controller is equivalent in function to the two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the ICH supports a serial interrupt scheme and also implements the I/O APIC controller. A table on [page 68](#) shows how the master and slave controllers are connected.

## 2 System Board

The Input/Output Controller Hub (82801AA)

### Timer/Counter Block

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval counter/timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.318 MHz oscillator input provides the clock source for these three counters.

### Advanced Programmable Interrupt Controller

Incorporated in the ICH, the APIC can be used in either single-processor or multi-processor systems, while the standard interrupt controller supports only single-processor systems.

### Real Time Clock

The RTC is 146818A-compatible, with 256 bytes of CMOS. The RTC performs two key functions: keeping track of the time of day and storing system data.

The RTC operates on a 32.768 kHz crystal and a separate 3V lithium battery that provides up to 7 years of protection for an unplugged system. It also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other security information. Another feature is a date alarm allowing for a schedule wake-up event up to 30 days in advance.

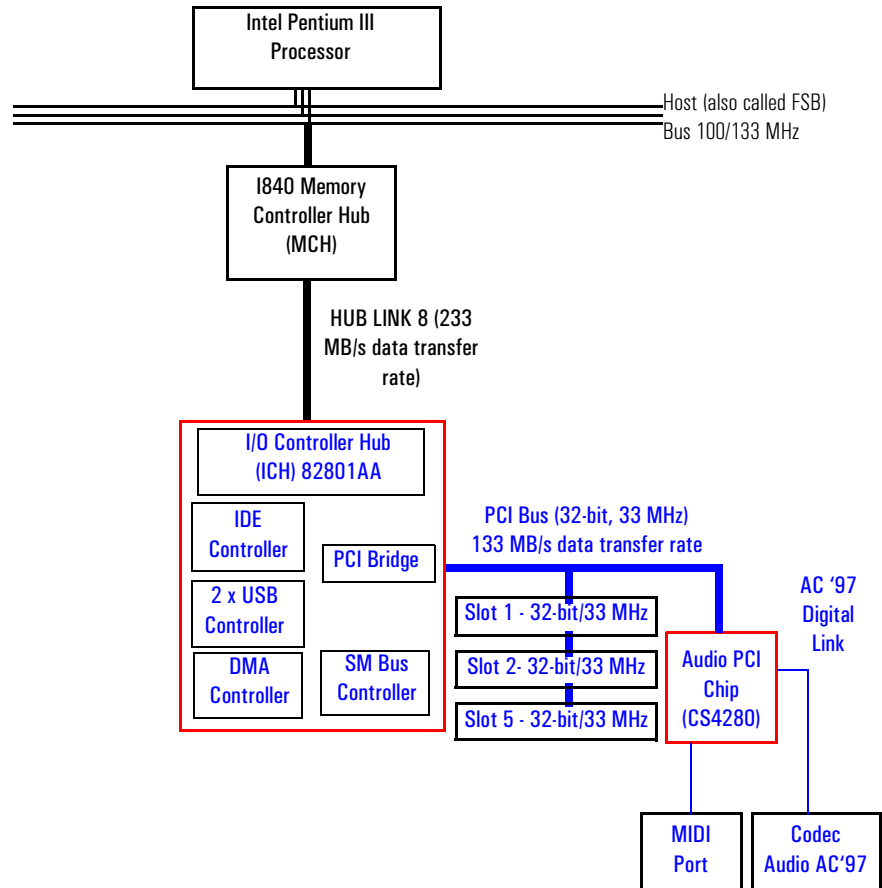
### Enhanced Power Management

The ICH's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states. A hardware-based thermal management circuit permits software-independent entry points for low-power states.

The ICH includes full support for the Advanced Configuration and Power Interface (ACPI) specifications.

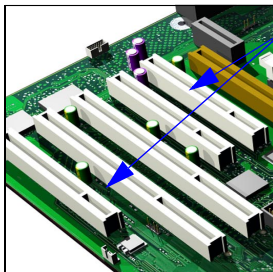
### Devices on the PCI 32-bit 33 MHz Bus

The following devices are connected to the PCI 32-bit 33 MHz bus.



#### PCI 32-bit/33 MHz Slots

There are three 32-bit/33 MHz PCI slots accepting 5 V PCI cards and Universal PCI cards (support for 3.3 V or 5 V). The LAN card should be installed in PCI Slot 5. PCI slots are explained in detail on [page 31](#).



## 2 System Board

The Input/Output Controller Hub (82801AA)

### Dual Chip PCI Audio Solution

The integrated PCI audio solution in the PC Workstation is a dual-chip solution made up of the CrystalClear™ CS4280 PCI audio controller and the CrystalClear CS4297 Audio Codec '97 (AC'97).

The CS4280 PCI audio controller interfaces with the PCI bus and performs all digital operations such as sample rate conversions and synthesis. The CS4297 AC'97 chip mixes and processes all the analog signals.

The interface between audio PCI chip and the audio codec is known as the AC'97 Digital Link.

#### CS4280 PCI Audio Interface Features

- PCI Version 2.1 Bus Master.
- Windows ® 95, Windows 98, Windows NT 4.0, Windows NT 2000 Drivers.
- Compliant with PC'99.
- MPU-401 interface, FM synthesizer, and Game Port.
- Full duplex operation.
- Advanced Power Management (PPMI).

#### CS4297 Audio Codec'97 Features

- AC'97 1.03 compatibility.
- Sophisticated mixed signal technology.
- 18-bit stereo full-duplex Codec with fixed 48kHz sampling rate.
- High quality differential CD input.
- Mono microphone input.
- Two analog line-level stereo inputs for LINE IN and CD (or VIDEO) connection.
- Single stereo line level output.
- Extensive power management support.
- Meets Microsoft's PC'99 audio performance requirements.

## Audio Chip Specifications

Feature	Description
<i>Digitized Sounds</i>	<ul style="list-style-type: none"> <li>• 16-bit and 8-bit stereo sampling from 4 kHz to 48 kHz.</li> <li>• Hardware Full Duplex Conversion.</li> <li>• 16-bit software-based real-time audio compression/decompression system.</li> </ul>
<i>Music Synthesizer</i>	<ul style="list-style-type: none"> <li>• Integrated OPL3 compatible music synthesizer.</li> </ul>
<i>Mixer</i>	<ul style="list-style-type: none"> <li>• MPC-3 audio mixer.</li> <li>• Input mixing sources: microphone, LINE In, CD Audio, AUX Audio, and digitized sounds.</li> <li>• Output mixing of all audio sources to the LINE Out or integrated PC Workstation speaker.</li> <li>• Multiple source recording and Left/Right channels balance.</li> </ul>
<i>Line Input</i>	<ul style="list-style-type: none"> <li>• Input impedance: 17k <math>\Omega</math> (ohms).</li> <li>• Input range: 0 to 2.83 Vpp</li> </ul>
<i>Line Output</i>	<ul style="list-style-type: none"> <li>• Stereo output of 100 mW per channel with headphone speakers (impedance 32 <math>\Omega</math>).</li> <li>• Output impedance: 570 <math>\Omega</math>.</li> <li>• Output range: 0 to 2.83 Vpp.</li> </ul>
<i>Microphone Input</i>	<ul style="list-style-type: none"> <li>• 20 dB gain preamplifier. The boost can be muted with software.</li> <li>• 32-level programmable volume control.</li> <li>• Input impedance: 600 <math>\Omega</math>.</li> <li>• Sensitivity: 30 mVpp to 283 mVpp.</li> </ul>
<i>Stereo Out Jack</i>	<ul style="list-style-type: none"> <li>• Impedance: 32 <math>\Omega</math>.</li> </ul>

## Devices on the SMBus

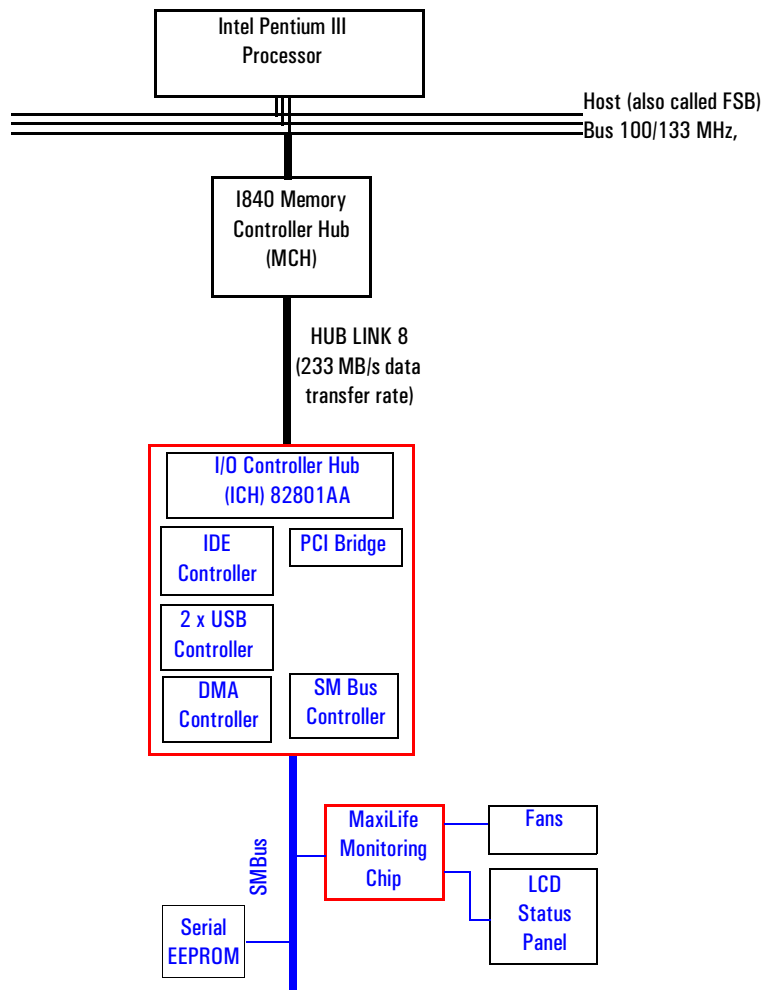
The SMBus is a subset of the I<sup>2</sup>C bus. It is a two-wired serial bus which runs at a maximum speed of 100 kHz. It is used to monitor some of the hardware functions of the system board (such as voltage levels, temperature, fan speed, memory presence and type), both at system boot and during normal run-time. It is controlled by the SMBus controller located in the ICH.

## 2 System Board

The Input/Output Controller Hub (82801AA)

The following devices are connected to the SMBus:

- LCD status panel.
- One Serial EEPROM MaxiLife (also includes backup values of CMOS settings).
- PCI slot 5, thus being ready for Alert-On LAN (AOL) from a hardware level.
- ICH SMBus Master Controller 100 kHz maximum.
- MaxiLife for hardware management, bus master controller.
- One LM75 thermal sensor on the system board.
- One ADM1024 hardware monitoring sensor.
- RIMM or DIMM serial EEPROM.





**ICH SMBus Master Controller**

The ICH provides a processor-to-SMBus controller. All access performed to the SMBus is done through the ICH SMBus interface. Typically, the processor has access to all the devices connected to the SMBus.

**DIMM Sockets**

Each DIMM socket is connected to the SMBus. The 168-pin DIMM modules include a 256 byte I<sup>2</sup>C Serial EEPROM. The first 128 bytes contain general information, including the DRAM chips' manufacturer name, DIMM speed rating, DIMM type, etc. The second 128 bytes of the Serial EEPROM can be used to store data online.

**RIMM Sockets**

Each RIMM socket is connected to the SMBus. The 168-pin RIMM modules include a 256 byte I<sup>2</sup>C Serial EEPROM. The first 128 bytes contain general information, including the DRAM chips' manufacturer name, RIMM speed rating, RIMM type, etc. The second 128 bytes of the Serial EEPROM can be used to store data online.

**ADM1024**

The ADM1024 chip is a hardware monitoring sensor dedicated to the processor temperature. This chip uses the thermal diodes integrated into each processor cartridge and makes the temperature information available through the SMBus. It also monitors processor power supply voltages.

**Serial EEPROM**

This is the non-volatile memory which holds the default values for the CMOS memory (in the event of battery failure). When installing a new system board, the Serial EEPROM will have a blank serial number field. This will be detected automatically by the BIOS, which will then prompt the user for the serial number which is printed on the identification label on the back of the PC Workstation. The computer uses 16KBytes of Serial EEPROM implemented within two chips. Serial EEPROM is ROM in which one byte at a time can be returned to its unprogrammed state by the application of appropriate electrical signals. In effect, it can be made to behave like very slow, non-volatile RAM. It is used for storing the tattoo string, the serial number, and the parameter settings for the *Setup* program as well as MaxiLife firmware.

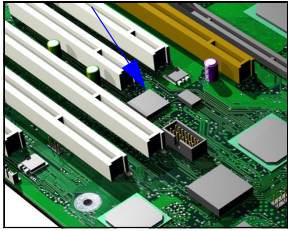
**LM75 Temperature Sensor**

The LM75 temperature sensor and alarm are located on the system board. The sensor is used to measure the temperature in various areas of the system board. This information is used to regulate fans.

## 2 System Board

The Input/Output Controller Hub (82801AA)

### HP MaxiLife Hardware Monitoring Chip



MaxiLife is a hardware monitoring chip which is resident on the system board. Its responsibility includes On/Off and reset control, status panel management (Lock button, LEDs), hardware monitoring (temperature and voltage), early diagnostics (CPU, memory, PLLs, boot start), run-time diagnostics (CPU errors), fan speed regulation, and other miscellaneous functions (such as special OK/FAIL symbols based on a smiling face).

The integrated microprocessor includes a Synopsys cell based on Dallas “8052” equivalent, a 2 KB boot ROM, 256 bytes of data RAM, an I<sup>2</sup>C cell, an Analog-to-Digital (ADC) with 5 entries, and an additional glue logic for interrupt control, fan regulation, and a status panel control.

MaxiLife downloads its code in 96 milliseconds from an I<sup>2</sup>C serial EEPROM. The total firmware (MaxiLife 8051-code, running in RAM) size is 14 KB. As it exceeds the 2 KB program RAM space, a paging mechanism will swap code as it is required, based on a 512 byte buffer. The first 2 KB pages of firmware code is critical because it controls the initial power on/reset to boot the system. This initial page is checked with a null-checksum test and the presence of MaxiLife markers (located just below the 2 KB limit).

MaxiLife is not accessible in I/O space or memory space of the system platform, but only through the SMBUS (which is a sub-set of the I<sup>2</sup>C bus), via the ICH. Its I<sup>2</sup>C cell may operate either in Slave or Master mode, switched by firmware, or automatically in the event of ‘Arbitration’ loss.

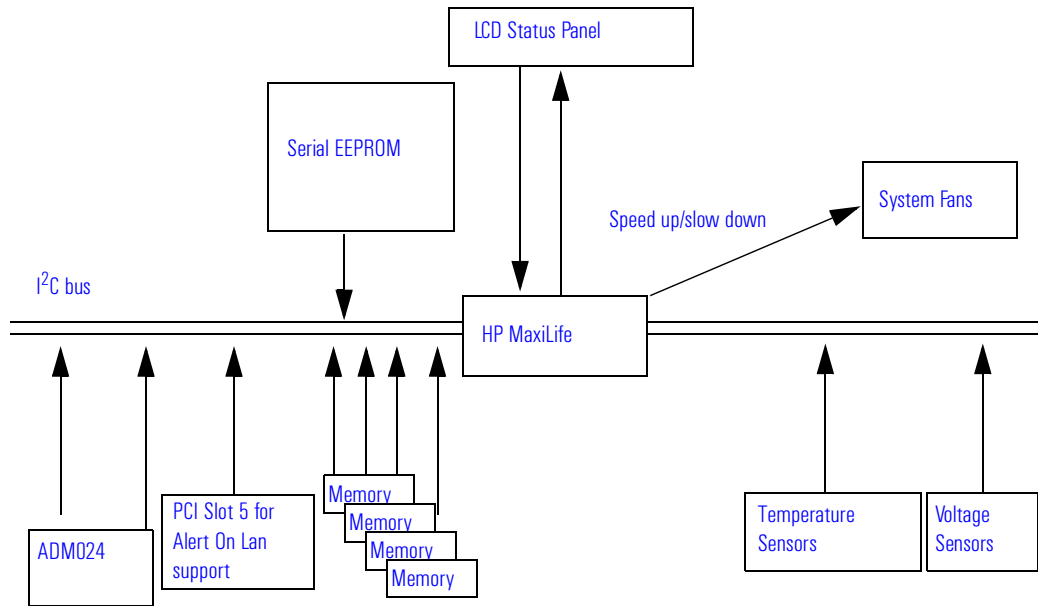
As a monitoring chip, MaxiLife reports critical errors at start-up, and is therefore powered by Vstandby (3.3V) power. For MaxiLife to work, the PC Workstation must be connected to a grounded outlet. This enables the PC Workstation’s hardware monitoring chip to be active, even if the system has been powered off.

### Test Sequence and Error Messages

Refer to [“MaxiLife Test Sequence and Error Messages” on page 107](#) for detailed information about the different test sequences and error messages

**MaxiLife Architecture**

The MaxiLife chip continuously monitors temperature and voltage sensors located in critical regions on the system board. This chip receives data about the various system components via a dedicated I<sup>2</sup>C bus, which is a reliable communications bus to control the integrated circuit boards.



**NOTE**

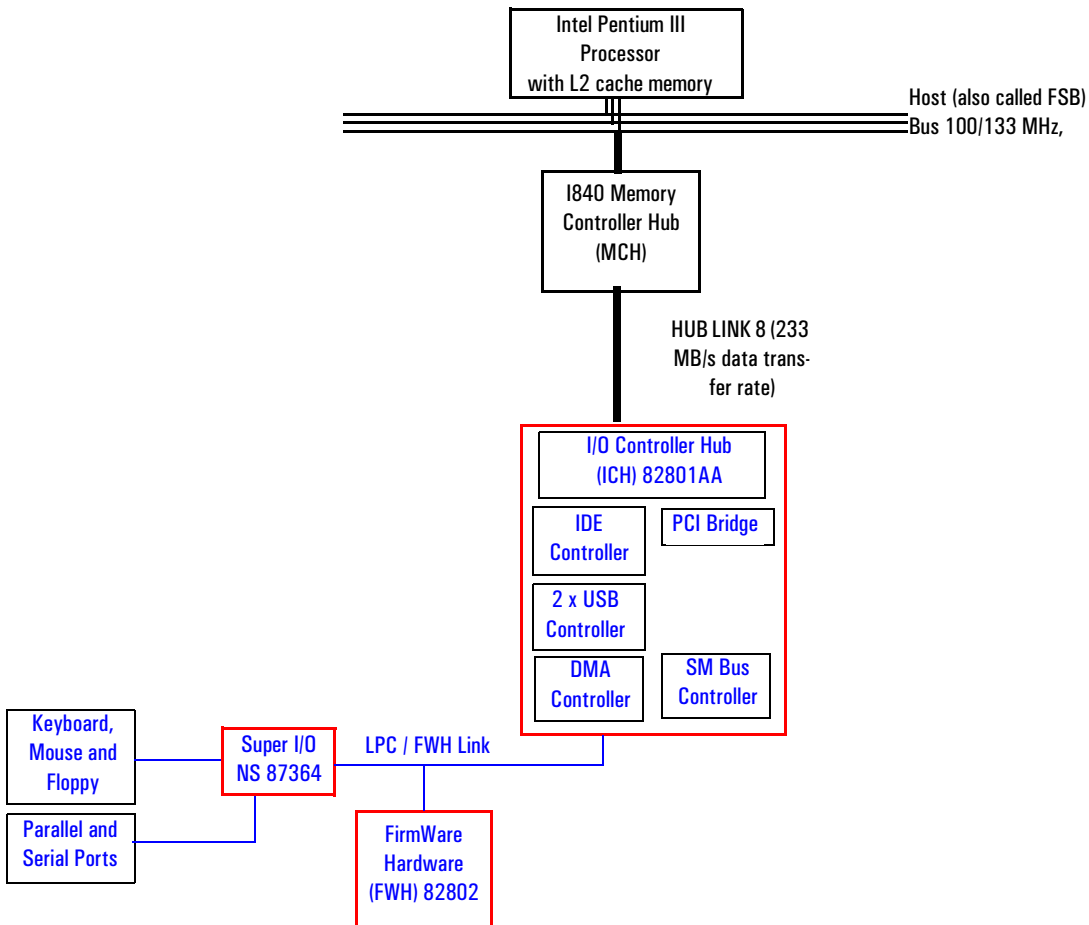
MaxiLife is powered by VSTBY. This means that it is functional as soon as the power cord is plugged in.

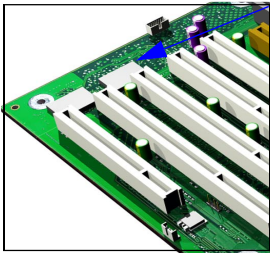
## 2 System Board

The Input/Output Controller Hub (82801AA)

### Devices on the Low Pin Count Bus

The following devices are connected to the LPC bus.





### The Super I/O Controller (NS 87364)

The *Super I/O* chip (NS 87364) provides the control for two FDD devices, two serial ports, one bidirectional multi-mode parallel port and a keyboard and mouse controller.

Device	Index	Data
Super I/O	2Eh	2Fh

### Serial / Parallel Communications Ports

The 9-pin serial ports (whose pin layouts are depicted on [page 138](#)) support RS-232-C and are buffered by 16550A UARTs, with 16-Byte FIFOs. They can be programmed as COM1, COM2, COM3, COM4, or disabled.

The 25-pin parallel port (also depicted on [page 139](#)) is Centronics compatible, supporting IEEE 1284. It can be programmed as LPT1, LPT2, or disabled. It can operate in the four following modes:

- Standard mode (PC/XT, PC/AT, and PS/2 compatible).
- Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible).
- Enhanced mode (enhanced parallel port, EPP, compatible).
- High speed mode (MS/HP extended capabilities port, ECP, compatible).

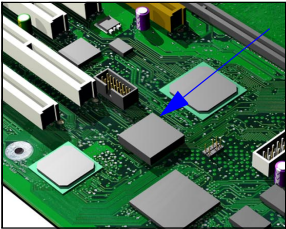
### FDC

The integrated *floppy disk controller* (FDC) supports any combination of two of the following: tape drives, 3.5-inch flexible disk drives, 5.25-inch flexible disk drives. It is software and register-compatible with the 82077AA, and 100% IBM-compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

### Keyboard and Mouse Controller

The computer has an 8042-based keyboard and mouse controller. The connector pin layouts are shown on [page 137](#).

## FirmWare Hub (82802AB)



The FWH (also known as flash memory) is connected to the LPC bus. It contains 4 Mbit (512 kB) of flash memory.

The hardware features of the FWH include: a Random Number Generator (RNG), five General Purpose Inputs (GPI), register-based block locking and hardware-based locking. An integrated combination of logic features and non-volatile memory enables better protection for the storage and update of system code and data, adds flexibility through additional GPIs, and allows for quicker introduction of security/manageability features.

The following table shows the available FWH features.

Feature	Feature
<ul style="list-style-type: none"> <li>● Platform Compatibility:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> Enables security-enhanced platform infrastructure.</li> <li><input type="checkbox"/> Part of the Intel I840 chipset.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Two Configurable Interfaces:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> FirmWare Hub interface for system operation.</li> <li><input type="checkbox"/> Address/Address Multiplexed (A/A Mux) interface.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● FirmWare Hub Interface Mode:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> Five signal communication interface supporting x8 reads and writes.</li> <li><input type="checkbox"/> Register-based read and write protection for each code/data storage blocks.</li> <li><input type="checkbox"/> Five additional GPIs for system design and flexibility.</li> <li><input type="checkbox"/> A hardware RNG (Random Number Generator).</li> <li><input type="checkbox"/> Integrated CUI (Command User Interface) for requesting access to locking, programming and erasing options. It also handles requests for data residing in status, ID and block lock registers.</li> <li><input type="checkbox"/> Operates with 33 MHz PCI clock and 3.3 V input/output.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● 4 Mbits of Flash Memory for system code/data non-volatile storage:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> Symmetrically blocked, 64 Kbyte memory sections.</li> <li><input type="checkbox"/> Automated byte program and block erase through an integrated WSM (Write State Machine).</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● A/A Mux Interface/Mode, supporting:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> 11-pin multiplexed address and 8-pin data I/O interface.</li> <li><input type="checkbox"/> Fast on-board or out-of-system programming.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Power Supply Specifications:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> Vcc: 3.3 V +/- 0.3 V.</li> <li><input type="checkbox"/> Vpp: 3.3 V and 12 V for fast programming, 80 ns.</li> </ul> </li> </ul>
<ul style="list-style-type: none"> <li>● Industry Standard Packages:                             <ul style="list-style-type: none"> <li><input type="checkbox"/> 40L TSOP or 32L PLCC.</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>● Case Temperature Operating Range.</li> </ul>

The FWH includes two hardware interfaces:

- FirmWare Hub interface.
- Address/Address Multiplexed (A/A Mux) interface.

The IC (Interface Configuration) pin on the FWH provides the control between these interfaces. The interface mode needs to be selected prior to power-up or before return from reset (RST# or INIT# low to high transition).

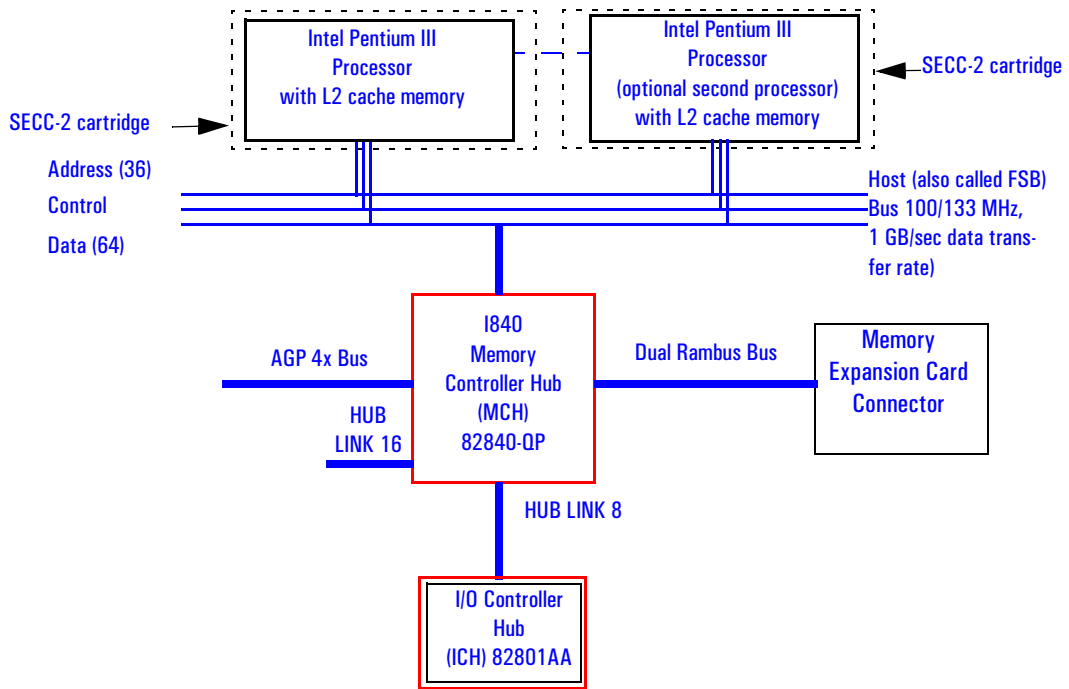
The FWH interface works with the ICH during system operation, while the A/A Mux interface is designed as a programming interface for component pre-programming.

An internal CUI (Command User Interface) serves as the control center between the FWH and A/A Mux interfaces, and internal operation of the non-volatile memory. A valid command sequence written to the CUI initiates device automation. An internal WSM (Write State Machine) automatically executes the algorithms and timings necessary for block erase and program operations.

## Host Bus

The Host bus of the Pentium III processors, also referred to as the FSB (Front Side Bus), is implemented in the GTL (Gunning Transceiver Logic)+ technology. This technology features open-drain signal drivers that are pulled-up to 1.5 V through resistors at bus extremities; these resistors also act as bus terminators, and are integrated in the processor.

If only one processor is installed, a terminating board must be installed in the second processor slot.



The supported operating frequencies of the GTL+ bus are 100 MHz or 133 MHz. The width of the data bus is 64 bits, while the width of the address is 36 bits. Along with the operating frequencies, the processor voltage is set automatically.

The control signals of the Host bus allow the implementation of a “*split - transaction*” bus protocol. This allows the Pentium III processor to send its request (for example, for the contents of a given memory address) and then to release the bus, rather than waiting for the result, thereby allowing it to



accept another request. The MCH, as target device, then requests the bus again when it is ready to respond, and sends the requested data packet. Up to eight transactions are allowed to be outstanding at any given time.

### Intel Pentium III Processor

The Pentium III processor has several features that enhance performance:

- Dual Independent Bus architecture, (supporting level cache sizes of i256 KB) plus a 64-bit system bus that enables multiple simultaneous transactions (refer to “*split -transaction*” above).
- MMX2 technology, which gives higher performance for media, communications and 3D applications.
- Dynamic execution to speed up software performance.
- Internet Streaming SIMD Extensions for enhanced floating point and 3D application performance.
- Processor Serial Number is an electronic number incorporated in the processor. If enabled, the Processor Serial Number can serve as a means of identifying the system. By default, this option is set to Disabled in the *Setup* program.
- Uses multiple low-power states, such as AutoHALT, Stop-Grant, Sleep and Deep Sleep to conserve power during idle times.

The Pentium III processor is packaged in a self-contained Single Edge Contact Cartridge (SECC-2) installed in a Slot 1 processor slot. The SECC-2 cartridge requires a 242-contact Slot 1 connector on the system board. It includes a processor core chip and GTL+ termination resistors.

There are two Slot 1 processor slots, along with one VRM (Voltage Regulation Module) socket. A single Pentium III processor for Slot 1 is powered through an onboard voltage regulator.

### Optional Second Processor

Single processor models can be upgraded to a dual processor system by installing a second processor in the vacant slot. The second processor must be a Pentium III processor for Slot 1 of the same speed as the first. The VRM supplied with the processor accessory kit is installed in the vacant VRM slot. The second processor is powered through the VRM.

## 2 System Board

### Host Bus

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**NOTE**

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When upgrading a processor or installing a second processor, the processor type and speed is automatically recognized by the BIOS. This means that no particular switch settings are required.

Upgrading a single processor to a dual processor system on Windows NT and Windows 2000 platforms is made easier with the HP DualExpress! application which is included in the HP processor application kit.

Installing a second processor is only advantageous when the software can make use of parallel activity. In particular, you need to be running a multi-threaded operating system that supports multiprocessing (one that is *SMP-ready*), such as Windows NT. The Windows NT operating system makes the best use of the Pentium III 32-bit architecture (though other operating systems will also show some benefit if 32-bit application programs are run).

The two processors must have the same speed.

### Configuring for Multi-Processing

*HP Kayak XU800 PC Workstations* support Symmetric Multi-Processing (SMP). When a second processor is added, it is automatically detected so there is no specific configuration required.

The “mono-processing” mode has been implemented in order to support operating systems that rely on the “legacy” interrupt controller 82C59 and are not aware of I/O APIC controller operation. Refer to [page 68](#) for further details.

### Processor Clock

The 100/133 MHz Host Bus clock is provided by a PLL. The processor core clock is derived from the Host Bus by applying a “fix ratio”.

### Bus Frequencies

There is a 14.318 MHz crystal oscillator on the system board. This frequency is multiplied to 133 MHz by a phase-locked loop. This is further scaled by an internal clock multiplier within the processor.

The bus frequency and the processor voltage are set automatically.

## Cache Memory

The cache memory is sealed within a single Pentium III package that contains the processor L1 and L2 cache.

The L1 cache memory has a total capacity of 32KB (16 KB data, 16 KB instructions). The L2 cache memory has a capacity of 256 KB, and is composed of four-way set-associative static RAM. Data is stored in lines of 32 bytes (256 bits). Thus two consecutive 128-bit transfers with the main memory are involved in each transaction.

TagRam and Burst-pipelined Synchronous Static RAM (BSRAM) memories are implemented on die. Transfer rates between the processor's core and L2 cache are at full processor core clock frequency and scale with the processor core frequency. Both the TagRam and BSRAM receive clocked data directly from the processor's core.

The amount of cache memory is set by Intel at the time of manufacture, and cannot be changed.

## 2 System Board

### Assigned Device Interrupts

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## Assigned Device Interrupts

### Input/Output Controller Hub Interrupts

Device	Reference Name	REQ/GNT	ID	IDSEL AD[xx]	Chip-set Interrupt Connection			
					INTA	INTB	INTC	INTD
AC'97 Audio Controller	CS4280	4 (ICH)	5	21	—	A	—	—
USB Controller	—	—	—	—	A	—	—	—
AGP slot	J34	—	0	16	A	B	—	—
PCI 32-bit slot #1	J37	1 (ICH)	6	22	C	D	A	B
PCI 32-bit slot #2	J38	0 (ICH)	8	24	A	B	C	D
PCI 32-bit slot #5 (LAN card)	J42	5 (ICH)	11	27	B	C	D	A

### PCI 64-bit Hub Interrupts

Device	Reference Name	REQ/GNT	ID	IDSEL AD[xx]	Interrupt Requests (IRQ)								
					0	1	2	3	4	5	6	7	8
Ultra-wide SCSI U160 Controller	AIC-7892	2 (P64H)	9	25	—	—	—	—	—	—	—	—	A
PCI 64-bit slot #3	J39	1 (P64H)	4	20	—	—	—	—	A	B	C	D	—
PCI 64-bit slot #4	J40	0 (P64H)	7	23	A	B	C	D	—	—	—	—	—

### Interrupt Controllers

The system has an Interrupt controller which is equivalent in function to that of two 82C59 interrupt controllers. The following table shows how the interrupts are connected to the APIC controller. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave (both of 82C59 type).

Although the *Setup* program can be used to change some of the settings, the following address map is not completely BIOS dependent, but is determined partly by the operating system. Note that some of the interrupts are allocated dynamically.

Interrupt Source	APIC Controller		Interrupt Signalling on	
	of device	Input	(PIC mode) <sup>1</sup>	(APIC modes)
INTA - PCI slot 3 (64/66)	P64H	IRQ0	BT_INT	APIC bus
INTB - PCI slot 3 (64/66)	P64H	IRQ1	BT_INT	APIC bus
INTC - PCI slot 3 (64/66)	P64H	IRQ2	BT_INT	APIC bus
INTD - PCI slot 3 (64/66)	P64H	IRQ3	BT_INT	APIC bus
INTA - PCI slot 4 (64/66)	P64H	IRQ4	BT_INT	APIC bus
INTB - PCI slot 4 (64/66)	P64H	IRQ5	BT_INT	APIC bus
INTC - PCI slot 4 (64/66)	P64H	IRQ6	BT_INT	APIC bus
INTD - PCI slot 4 (64/66)	P64H	IRQ7	BT_INT	APIC bus
INTA - onboard SCSI controller	P64H	IRQ8	BT_INT	APIC bus
AGP - INTA, PCI Slot 1 - INTC, PCI Slot 2 - INTA, PCI Slot 5 - INTB	ICH	INTA	INT	APIC bus
PCI Audio - INTA, AGP - INTB, PCI Slot 1 - INTD, PCI Slot 2 - INTB, PCI Slot 5 - INTC	ICH	INTB	INT	APIC bus
BT_INT, PCI Slot 1 - INTA, PCI Slot 2 - INTC, PCI Slot 5 - INTD	ICH	INTC	INT	APIC bus
USB - INTA, PCI Slot 1 - INTB, PCI Slot 2 - INTD, PCI Slot 5 - INTA	ICH	INTD	INT	APIC bus
Device on Primary IDE Channel	ICH	IRQ14	INT	APIC bus
Device on Secondary IDE Channel	ICH	IRQ15	INT	APIC bus
Serial Interrupt from Super I/O	ICH	SERIRQ	INT	APIC bus

<sup>1</sup>. In PIC mode, the Interrupts signaled to the P64H are chained as INTC to the ICH.

There are three major interrupt modes available:

*PIC mode*: This mode uses only the “Legacy” interrupt controllers, so that only one processor can be supported. Because this system has dual processor capability, this mode is not chosen by default by Windows NT. However, during Windows NT installation, you have the possibility of selecting this mode.

## 2 System Board

### Assigned Device Interrupts

*Virtual wire mode:* This mode is implemented with APIC controllers in the ICH and P64H and used during boot time. The virtual wire mode allows the transition to the “symmetric I/O mode”. In the virtual wire mode, only one processor executes instructions.

*Symmetric I/O mode:* This mode is implemented with APIC controllers in the ICH and P64H, and allows for multiple processor operations.

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**NOTE**

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In “PIC mode” and “virtual wire mode”, the PCI interrupts are routed to the INT line. In the “symmetric I/O mode”, the PCI interrupts are routed to the I/O APIC controllers and forwarded over an APIC bus to the processors.

### PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

PCI interrupts can be shared; several devices can use the same interrupt. However, optimal system performance is reached when minimizing the sharing of interrupts. Refer to [page 68](#) for a table of the PCI device interrupts.

## Interface Cards

This chapter describes the graphics and network devices that are supplied with the PC Workstation.

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### Graphics Cards

*HP Kayak XU800 PC Workstation* models are supplied with a graphics card. This graphics card is one of the following, depending on the PC Workstation model:

- Matrox Millennium G250.
- Matrox Millennium G400.
- 3Dlabs Oxygen GVX1.
- ELSA Synergy™ II.

#### Matrox Millennium G250 Graphics Card

The Matrox Millennium G250 graphics card has a total of 8 MB of installed video memory, which can be upgraded to a maximum of 16 MB.

The Matrox Millennium G250 on-board MGA G-250 processor communicates directly with the Pentium II processor along the AGP 2X bus. The controller can be characterized as follows:

- Supports full AGP 2X mode
- Graphics controller in 272-pin BGA (Ball Grid Array) package
- Integrated 64-bit, 250 MHz RAMDAC
- New, high-performance triangle setup engine to off-load system CPU
- Improved 3D drawing engine supports:
  - Bilinear texture filtering
  - Fogging.
  - Alpha blending
  - Anti-aliasing
  - Specular highlighting

### 3 Interface Cards

#### Graphics Cards

- High-performance VGA
- Integrated front-end and back-end scalers
- Fully Direct Draw, Direct 3D, Mini Client Drivers (MCD), and OpenGL<sup>®</sup> compliant
- 143 MHz SGRAM (LVTTL) memory configurations (up to 16 MB maximum)
- Support for memory upgrade via 144-pin SO\_DIMM memory modules (SGRAM)
- Serial EEPROM video BIOS interface (32 KB)
- ITU-656 and VMI-like host port provides interface to low-cost decoders/CODECs
- 12-bit digital RGB port (MAFC) provides support for video encoders and panel link interfaces

The diagram below shows the Matrox Millennium G250 graphics card .



#### Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.



The tables below summarize the video resolutions and refresh rates that are supported.

<b>Resolution 2D/3D</b>	<b>8-bit 256 colors</b>	<b>16-bit 64k colors</b>	<b>24-bit 16.7 million colors</b>	<b>32-bit 16.7 million colors</b>
640x480	200 Hz	200 Hz	200 Hz	200 Hz
800x600	180 Hz	180 Hz	180 Hz	180 Hz
1024x768	140 Hz	140 Hz	140 Hz	140 Hz
1152x864	120 Hz	120 Hz	120 Hz	120 Hz
1280x1024	100 Hz	100 Hz	100 Hz	90 Hz
1600x1200	90 Hz	90 Hz	85 Hz	65 Hz
1800x1440	80 Hz	80 Hz	75 Hz	65 Hz
1920x1440	76 Hz	76 Hz	70 Hz	-
2048x1536	70 Hz	70 Hz	65 Hz	-

<b>Maximum Refresh Rates<sup>1</sup></b>			
<b>Resolution</b>	<b>8 bpp / 16 bpp</b>	<b>24 bpp</b>	<b>32 bpp</b>
640x480	200 Hz	200 Hz	200 Hz
800x600	180 Hz	180 Hz	180 Hz
1024x768	140 Hz	140 Hz	140 Hz
1152x864	120 Hz	120 Hz	120 Hz
1280x1024	100 Hz	100 Hz	90 Hz
1600x1200	90 Hz	85 Hz	65 Hz
1920x1080	80 Hz	80 Hz	60 Hz
1920x1200	76 Hz	70 Hz	-
1800x1440	70 Hz <sup>2</sup>	65 Hz	-

<sup>1.</sup> Your display may not support the maximum refresh rates shown here. Refer to the User's Guide supplied with your display for details of the refresh rates supported by your display.

<sup>2.</sup> Limitation due to 250 MHz RAMDAC.

### 3 Interface Cards

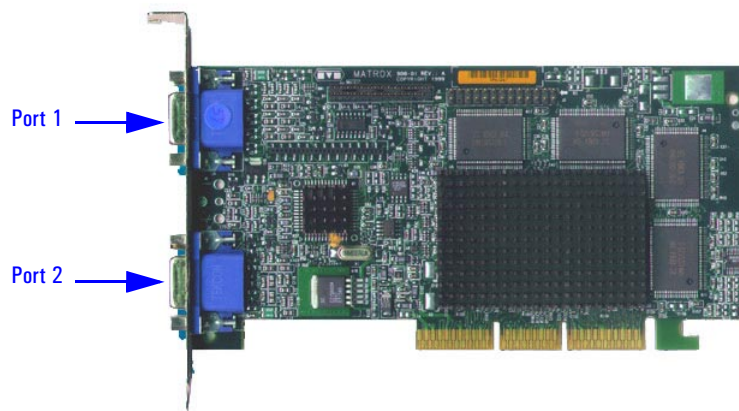
#### Graphics Cards

#### Matrox Millennium G400 Graphics Card

The Matrox Millennium G400 Dual AGP 2X/4X graphics card has 16MB of installed video memory (non-upgradeable), and can be characterized as follows:

- Powered by the Matrox MGA-G400 chip
- Full AGP 2X/AGP 4X support (up to 1GB/s bandwidth)
- Integrated 300MHz RAMDAC with Ultra Sharp technology for highly saturated and separated colors
- Matrox DualHead Display technology with PowerDesk desktop manager:
  - Easy multiple resolutions support
  - Simple dialog box
  - Effortless multiple-window management
- DDC2B support for Plug & Play detection of monitor
- 256-bit dual bus architecture; true 128-bit external bus to video memory
- Vibrant color quality - true 32-bit ARGB
- Supports 32-bit Z buffering for exceptional rendering precision
- 32-bit internal precision specially enhanced for multi-texturing using 32-bit text sources
- 16/10 monitor support
- Support for true 32-bit color (16.7 million colors) at resolutions of up to 2048 x 1536
- Bilinear, trilinear, and anisotropic filtering
- Floating-point 3D setup engine
- DirectX 6 and OpenGL<sup>®</sup> compliant

The diagram below shows the Matrox Millennium G400 graphics card .




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**NOTE**

If only one monitor is used, then Port 1 must be used.

In the case where a second monitor is installed, it is detected by the driver during the operating system boot (not after).

If only one monitor is detected, then only the mono head settings will be available in the Driver Configuration screens.

---

### Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

The tables below summarize the 2D and 3D video resolutions that are supported, and the refresh rates.

Color palette	Max. 2D display area	Max. 3D display area	Double-buffered + 16-bit Z	Double-buffered + 16-bit Z
8-bit	2048 x 1536			
15- or 16-bit	2048 x 1536	2048 x 1536	1880 x 1440	1600 x 1200
124-bit	2048 x 1536	-	-	-
32-bit	2048 x 1536	1600 x 1200	1280 x 1024	1280 x 1024

### 3 Interface Cards

#### Graphics Cards

<b>Maximum Refresh Rates</b>		
<b>Resolution (4:3 aspect ratio)</b>	<b>Main Display (8-/16-/24-/32-bit)</b>	<b>Second Display (16-/32-bit)</b>
640x480	200 Hz	200 Hz
800x600	200Hz	180 Hz
1024x768	160 Hz	115 Hz
1152x864	140 Hz	95 Hz
1280x1024	120 Hz	75 Hz
1600x1200	100 Hz	43 Hz
1600x1280	90 Hz	43 Hz
1800x1440	80Hz	-
1920x1440	75 Hz	-
2048x1536	70Hz	-
<b>Resolution (16:9 aspect ratio)</b>	<b>Main Display (8-/16-/24-/32-bit)</b>	<b>Second Display (16-/32-bit)</b>
1600x1024	120 Hz	43
1920x1035	100 Hz	-
1920x1080	100 Hz	-
1920x1200	90 Hz	-

### 3Dlabs Oxygen GVX1

There is a total of 32 MB of video Synchronous Graphics RAM (SGRAM) memory installed on the graphics card .

#### Features

- OpenGL-based geometry and lighting acceleration entirely in the hardware, freeing the processor for other applications
- OpenGL specific extensions that double the performance under AutoCad
- Innovative virtual textures technology, using on-board graphics memory to cache large textures
- Multi-screen support (with additional PCI cards)
- Supports 16: 10 wide-format monitors
- PowerThreads™ SSE OpenGL drivers fully tested with all leading professional graphics applications

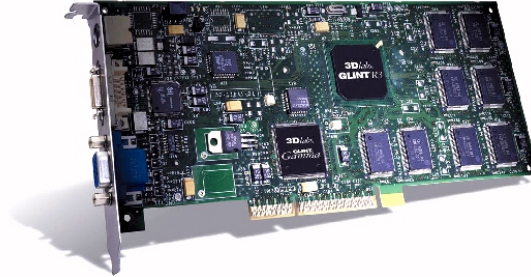
#### Specifications

- Full AGP 1X support
- Professional 3D rendering features that include:
  - Perspectively correct bilinear and trilinear filtering
  - Perspectively correct per-pixel MIP mapping
  - Single pass dual bilinear mip-mapped textures
  - Flat and Gouraud shading
  - Source and destination Alpha blending for transparency
  - High-quality anti-aliasing
  - Fog and depth-cueing
  - Overlay and stencil buffers
  - 32-bit Z-buffering
  - GID clipping
- GLINT R3 Rasterization processor for:
  - Virtual texture memory management unit
  - Up to 256 MB virtual texture address space
  - Integrated 300MHz RAMDAC
  - High-speed 128-bit memory interface
  - 2D/3D raster engine
  - Integrated SVGA controller

### 3 Interface Cards

#### Graphics Cards

The diagram below shows the 3Dlabs Oxygen GVX1 graphics card .



#### Video Memory

The video memory, also known as SGRAM, is a local block of RAM for holding major data structures: Frame Buffer (double buffer), Z-Buffer and T-Buffer (Texture Buffer). The Frame Buffer holds one frame steady on the screen while the next one is being processed, while the Z-buffer stores depth information for each pixel.

#### Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display. The table below summarizes the 3D video resolutions and refresh rates that are supported.

Display resolution	Color depth	Refresh rates
640 x 480	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
800 x 600	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1024 x 768	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1152 x 864	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1280 x 960	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1280 x 1024	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1600 x 1200	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1920 x 1080	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1920 x 1200	8-bit, 16-bit, True color	76 Hz
2048 x 1536	8-bit, 16-bit, True color	60 Hz

## ELSA Synergy II Graphics Card

The ELSA Synergy™ II graphics card has 32 MB of Synchronous Graphics RAM (SGRAM) installed video memory.

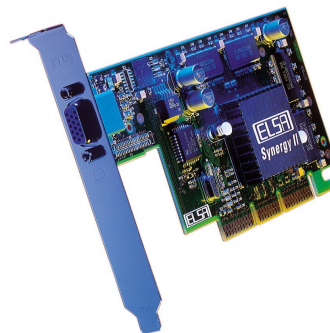
### Features

- Fastest 128-bit 2D performance
- 3D hardware texture acceleration
- Resolution support up to 1920 x 1200 at 96 Hz
- Multi-screen support (up to 4 with additional PCI cards)
- Supports 16: 10 wide-format monitors
- Software tools: ELSA POWERdraft, ELSA MAXtreme, ELSA Views3D
- OpenGL® extensions for AutoCAD 2000 that doubles performance
- PowerThreads™ SSE OpenGL drivers fully tested with all leading professional graphics applications

### Specifications

- Full AGP 2X/AGP 4X support
- RIVA TNT2 (NVIDIA) graphics processors
- VESA 3 (flash ROM)
- Integrated 300 MHz RAMDAC
- 3D standards: Hardware accelerated OpenGL®, DirectX3, DirectX5/6
- Standards: VESA DPMS, DDC2B, Plug & Play

The diagram below shows the ELSA Synergy II graphics card .



### 3 Interface Cards

#### Graphics Cards

#### Video Memory

The video memory, also known as SGRAM, is a local block of RAM for holding major data structures: Frame Buffer (double buffer), Z-Buffer and T-Buffer (Texture Buffer). The Frame Buffer holds one frame steady on the screen while the next one is being processed, while the Z-buffer stores depth information for each pixel.

#### Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

The table below summarizes the 3D video resolutions and refresh rates that are supported.

Display resolution	Color depth	Refresh rates
640 x 480	8-bit, 16-bit, True color	200, 100, 85, 75, 60 Hz
800 x 600	8-bit, 16-bit, True color	200, 100, 85, 75, 60 Hz
1024 x 768	8-bit, 16-bit, True color	200, 100, 85, 75, 60 Hz
1152 x 864	8-bit, 16-bit, True color	200, 100, 85, 75, 60 Hz
1280 x 960	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1280 x 1024	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1600 x 1200	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1920 x 1080	8-bit, 16-bit, True color	100, 85, 75, 60 Hz
1920 x 1200	8-bit, 16-bit, True color	up to 96 Hz

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**NOTE**

200 Hz accepted if supported by the monitor.



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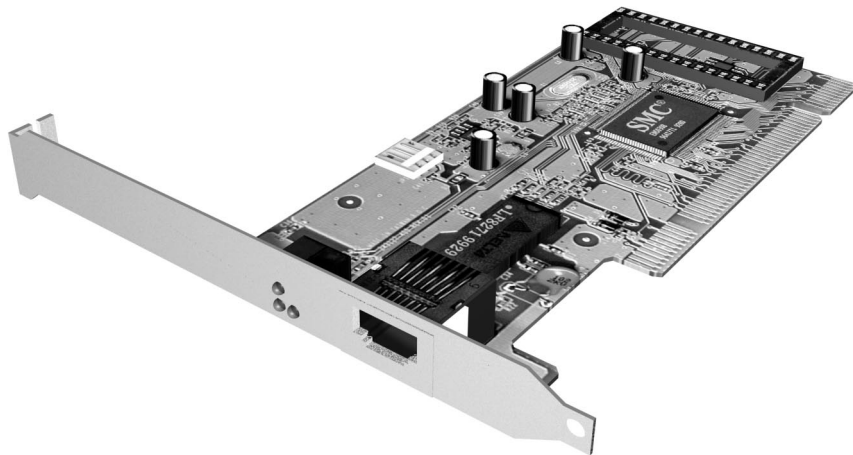
## Network Cards

Most *HP Kayak XU800 PC Workstation* models are supplied with an HP 10/100 TX LAN card.

A description and features of other supported LAN cards are also mentioned in this section.

### HP 10/100 TX PCI LAN Interface

The 10/100 TX LAN Interface is a 32-bit PCI 2.2 card that supports 10 Mbits per second (10 BaseT) and 100 Mbits per second (100 TX) transfer speeds, and both half and full duplex operation.



### 3 Interface Cards

#### Network Cards

#### HP 10/100 TX PCI LAN Interface Features

Feature:	Description:
<i>RJ45 Connector</i>	Connection to Ethernet 10/100 TX autonegotiation
<i>BootROM</i>	Protocols: <ul style="list-style-type: none"> <li>• PxE 2.0,</li> <li>• On-board socket support up to 128 Kb.</li> </ul>
<i>Remote Power On (RPO)</i>	Full remote power on using Magic Packet for Microsoft Windows 95, Windows 98, Windows NT4 in APM mode.
<i>Remote Wake Up (RWU)</i>	Enable and Wake Up from Suspend state using Magic Packet and Pattern Matching for Microsoft Win98SE and Win2000 in ACPI mode.  This feature enables a host computer to remotely (over the network) power on computers and wake computers up from energy-saving Sleep mode. For these features to work, use the Setup program to configure the BIOS.
<i>Power Management</i>	<ul style="list-style-type: none"> <li>• OnNow 1.0,</li> <li>• Advanced Power Management 1.2,</li> <li>• PCI Power Management 1.1,</li> <li>• WfM 2.0 compliant, ACPI.</li> </ul>
<i>Manageability</i>	<ul style="list-style-type: none"> <li>• Desktop Management Interface (DMI) 2.0 Dynamic driver,</li> <li>• DMI 2.0 SNMP mapper,</li> <li>• PXE 2.0 Flashable BootROM (optional on socket).</li> </ul>
<i>Diagnostic</i>	<ul style="list-style-type: none"> <li>• Mac address DOS report tool,</li> <li>• User Diag for DOS.</li> </ul>

#### HP 10/100 TX PCI LAN Interface LED Descriptions

LED	Description	Flashing	Steady	Off
<i>10 LNK</i>	Link integrity	Reversed polarity	Good 10 Base-T connection between NIC and hub.	No connection between NIC and hub
<i>100 LNK</i>	Link integrity	Reversed polarity	Good 100 TX connection between NIC and hub.	No connection between NIC and hub
<i>ACT</i>	<b>Yellow:</b> Port traffic for either speed	Network traffic present	Heavy network traffic	No traffic

## Supported LAN Cards

The following LAN cards are supported on the *HP Kayak XU800 PC Workstation*.

### 3COM NIC (Network Interconnect) LAN Card

#### 3COM NIC LAN Card Features

Feature	Description
<i>Interface</i>	32-bit 10/100 BT full duplex RJ LAN Port.
<i>LED</i>	Three LEDs: <ul style="list-style-type: none"> <li>• activity,</li> <li>• 10 MB/s speed,</li> <li>• 100 MB/s speed.</li> </ul>
<i>Labels</i>	PCI 2.2 Specification, PC 99, Intel WfM 2.0.
<i>Power Management</i> <sup>1</sup>	<ul style="list-style-type: none"> <li>• RPO and RWU for APM Windows 95 and Windows 98,</li> <li>• RWU for ACPI Windows 98 and Windows 2000,</li> <li>• RPO for Windows NT 4,</li> <li>• OnNow 1.0, APM 1.2,</li> <li>• PCI power management. 1.1,</li> <li>• WOL, PCI VccAux 3.3 V.</li> </ul>
<i>Manageability</i>	DMI 2.0 Component Code.
<i>Diagnostic</i>	<ul style="list-style-type: none"> <li>• Mac address DOS report tool,</li> <li>• User Diag for DOS, Windows NT 4, Windows 95 and Windows 98.</li> </ul>
<i>Drivers</i>	Major OSes, Minor OSes.
<i>Boot ROM</i>	Multiboot BootROM (BIOS or socket).
<i>Remote Wake Up (RWU)</i>	This feature enables a host computer to remotely (over the network) power on computers and wake computers up from energy-saving Sleep mode. For these features to work, use the Setup program to configure the BIOS.

### 3 Interface Cards

#### Network Cards

#### 3COM LAN Card LED Descriptions

LED	Description	Flashing	Steady	Off
<i>10 LNK</i>	<b>GREEN:</b> Link integrity	Reversed polarity	Good 10 Base-T connection between NIC and hub.	No connection between NIC and hub
<i>100 LNK</i>	<b>GREEN:</b> Link integrity	Reversed polarity	Good 100 TX connection between NIC and hub.	No connection between NIC and hub
<i>ACT</i>	<b>Yellow:</b> Port traffic for either speed	Network traffic present	Heavy network traffic	No traffic

## INTEL NIC (Network Interconnect) LAN Card

### INTEL NIC LAN Card Features

Feature	Description
<i>Interface</i>	IEEE802.3 100 Base-TX, IEEE802.3 10 Base-T, 32-bit 10/100 BT full duplex RJ LAN Port.
<i>LED</i>	Two LEDs: <ul style="list-style-type: none"> <li>• one for act/lnk (activity and link),</li> <li>• one for 10 MB operation (on = 100 MB, off = 10MB).</li> </ul>
<i>Labels</i>	PCI 2.2 Specification, PC 99.
<i>Power Management</i>	<ul style="list-style-type: none"> <li>• Wfm 2.0 compliant,</li> <li>• RPO and RWU for APM Windows 95 and Windows 98,</li> <li>• OnNow 1.0, APM 1.2,</li> <li>• PCI power management 1.1,</li> <li>• VccAux s3.3 V support via PCI bus 2.2,</li> <li>• VccAux 5 V support via 3-pin WOL.</li> </ul>
<i>Manageability</i>	DMI 2.0 and DMI 2.0 SNMP mapper.
<i>Diagnostic</i>	<ul style="list-style-type: none"> <li>• Windows and DOS based,</li> <li>• Mac address DOS report tool,</li> <li>• User Diag for DOS, Windows NT 4, Windows 95 and Windows 98.</li> </ul>
<i>Drivers</i>	Major OSes, Minor OSes.
<i>Boot ROM</i>	Onboard flash ROM.
<i>Remote Wake Up (RWU)</i>	This feature enables a host computer to remotely (over the network) power on computers and wake computers up from energy-saving Sleep mode. For these features to work, use the Setup program to configure the BIOS.

### INTEL NIC LAN Card LED Descriptions

LED	On	Flashing	Off
<i>ACT/LNK</i>	Adapter and hub are receiving power. Cable connection is good.	Receiving or sending packets	Adapter and hub are not receiving power. Cable connection could be faulty or there is a driver configuration problem.
<i>100 TX</i>	Operating at 100 Mbps	N/A	Operating at 10 Mbps

### 3 Interface Cards

Network Cards

## Mass Storage Devices

This chapter describes the mass storage devices that are supplied with the PC Workstation. Refer to the diagram on [page 13](#) for the position of the different mass storage devices in the PC Workstation. This chapter also summarizes the pin connections on internal and external connectors.

HP product numbers and replacement part numbers for mass storage devices are listed in the Service Handbook Chapter, which can be accessed from the HP World Wide Web site at the following address:

<http://www.hp.com/go/kayaksupport>.

### Flexible Disk Drives

A 3.5-inch, 1.44 MB flexible disk drive is supplied in the front-access shelf.

### Hard Disk Drives

The following table lists the 3.5-inch (1-inch high) hard disk drives (which are subject to change) that may be supplied (type and quantity depends on model) on internal shelves, connected to the SCSI or IDE controller.

	<b>Cheetah 18LP SCSI Seagate (10 krpm)</b>	<b>Atlas (Tornado) SCSI Quantum (10 krpm)</b>	<b>Barracuda IDE Seagate (7.2 krpm)</b>
Capacity	9.1 GB and 18 GB	9.1 GB and 18 GB	15 GB
Interface	Ultra2 Wide SCSI	Ultra160	UltraIDE ATA/66
External peak transfer rate	80 MB/s	160 MB/s	66 MB/s
Average seek time (read)	5.4 ms	5.4 ms	7.6 ms
Internal formatted transfer rate (MB/s)	29.5 max.	20 to 29	43
Number of discs/heads	9.1 GB: 3/6 18 GB: 6/12	9.1 GB: 3/6 18 GB: 6/12	15 GB: 2/4
Buffer size	1 MByte	2 MBytes	512 KBytes

## CD-ROM Drives

**IDE 48X CD-ROM Drive** Some models<sup>1</sup> have a 48X IDE CD-ROM drive supplied in a 5.25-inch front-access shelf ATAPI, supporting ATAPI commands and with audio playback capability. It can play any standard CD-Audio disks, in addition to CD-ROM disks, conforming to optical and mechanical standards as specified in the Red, Yellow, Green and Orange Book.

Some of the 48X IDE CD-ROM features include:

- Application Disk type (confirmed by Red, Yellow, Green, Orange Book)
- CD-ROM data disk (Mode 1 and Mode 2)
- Photo-CD Multisession
- CD Audio disk
- Mixed mode CD-ROM disk (data and audio)
- CD-ROM XA, CD-I, CD-Extra, CD-R, CD-RW

	Description
Data capacity	650 MB
Data transfer rate	Sustained transfer rate (1X = 150 KB/s); Outerside: 7,200 KB/s Burst transfer rate: PIO mode 4 - 16.6 Mbytes/s maximum Single Word DMA Mode 2 - 8.3 Mbytes/s maximum Multi Word DMA Mode 2 - 16.6 Mbytes/s maximum
Buffer memory size	128 kbytes
Access time	Average Stroke (1 / 3) 110 ms Full Stroke 180 ms
Rotational speed	2,048 bytes (Mode-1) 2,336 bytes (Mode-2)
Interface	ATAPI
Power requirements	5V, 1.2A 12V, 0.8A

1. Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the 48X IDE CD-ROM.



**8X Video IDE DVD-ROM Drive**

Some models<sup>1</sup> have a DVD-ROM (Read Only) drive. It can play any standard CD-Audio disks, in addition to CD-ROM disks, conforming to optical and mechanical standards as specified in the Red, Yellow, Orange and Green Books.

	Description
Data capacity	650 MB
Data transfer rate	Sustained transfer rate (1X = 150 KB/s); Outerside: 7,200 KB/s Burst transfer rate: PIO mode 4 - 16.6 Mbytes/s maximum Single Word DMA Mode 2 - 8.3 Mbytes/s maximum Multi Word DMA Mode 2 - 16.6 Mbytes/s maximum
Buffer memory size	128 kbytes
Access time	Average Stroke (1 / 3) 110 ms Full Stroke 180 ms
Rotational speed	2,048 bytes (Mode-1) 2,336 bytes (Mode-2)
Interface	ATAPI
Power requirements	5V, 1.2A 12V, 0.8A

1. Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the DVD-ROM drive.

**4X IDE CD-Writer Plus Drive**

Some models<sup>1</sup> have a CD-RW (ReWritable) drive supplied in a 5.25-inch front-access shelf ATAPI, supporting ATAPI commands and with audio playback capability. It can play any standard CD-Audio disks, in addition to CD-ROM disks, and can record both write-once (CD-R) and CD-RW optical media. It conforms to optical and mechanical standards as specified in the Red, Yellow, Orange and Green Books.

	Description
Data capacity	650 MB or up to 74 minutes of audio per disc 547MB in CD-UDF data format
Performance	Seek time (1/3 stroke: < 150 ms (CD-ROM)) Data transfer rate: Read: Up to 24X (1X = 150 KB/s) Write: 4X (CD-R); 2X (CD-RW)
Minimum burst transfer rate	2.5Mbytes/sec.
Spin-up time (2X)	2 seconds max. (from spin down state until disc ready)
Initialization time (2X)	5 seconds max. (from new disc inserted until disc ready)
HP fast format time (CD-RW)	5 minutes max.
Disc finalization time (2X)	2 minutes typical
Corrected error rate	Audio, Mode 2, Mode 2 Form 2: < 1 frame in 10 <sup>9</sup> bits read Mode 1, Mode 2 Form 1: < 1 frame in 10 <sup>12</sup> bits read
Buffering	1MByte (> 6 sec at 1X speed). If buffered data drops to less than one sector, the recording stops.
Write methods	- Track at once - Disc at once - Incremental (packet) - Multisession
Write verification	Automatic Power Control to dynamically adjust laser writer power
Format and EEC standard	Red, Yellow, Orange, Green books
MTBF	150,000 hours
Interface	ATAPI

1. Refer to the HP Kayak PC Workstations Service Handbook to find out which models are installed with the HP CD-RW drive.

---

## HP BIOS

The *Setup* program and BIOS are summarized in the two sections of this chapter. The POST routines are described in the next chapter.

The BIOS is based on an AMIBIOS® core, which includes support for 4 M/bits flash parts, PCI 2.2 Specification, and RIMM or DIMM memory modules. Added to this, a New BIOS Architecture (NBA) has been implemented. The main principle of the NBA is that HP features are independent modules and run at defined moments in the boot process. They are installed as hooks, either in:

- *Source code form*, for small tasks, or before memory is available.
- *Binary*. As .COM files, for larger tasks once memory is available.

They both communicate with the BIOS through CMOS and memory tables providing information to the operating system through SMBIOS tables.

So, what are hooks? Hooks are architected points in the BIOS where specific code can be run. HP code is integrated, as mentioned above, in either source/object files, or as separate binaries.

---

## HP/NBA BIOS Summary

The System ROM contains the POST (Power-On-Self-Test) routines and the BIOS: the System BIOS, video BIOS, and low option ROM. This chapter, together with the following one, give an overview of the following aspects:

- Menu-driven *Setup* with context-sensitive help, described next in this chapter.
- The address space, with details of the interrupts used, described at the end of this chapter.
- The Power-On-Self-Test or POST, which is the sequence of tests the computer performs to ensure that the system is functioning correctly, described in the next chapter.

The system BIOS is identified by the version number *qXX.YM.mm*, where:

- *q* is an optional letter indicating non-production status (removed at release).
- *XX* is a two-letter code indicating the system (IA).
- *Y* is a one-digit code indicating the HP entity.
- *M* is the major BIOS version.
- *mm* is the minor BIOS version.

## 5 HP BIOS

### HP/NBA BIOS Summary

An example of a released version would look similar to the following example: IA.11.02.

The procedure for updating the System ROM firmware is described on [page 95](#).

### Using the HP *Setup* Program

To run the *Setup* program, press **(F2)** while the initial “Kayak” logo is displayed immediately after restarting the PC.

Alternatively, press **(Esc)** to view the summary configuration screen. The summary screen will remain visible until a key is pressed.

The band along the top of the *Setup* screen offers the following menus: Main, Advanced, Security, Boot, Power and Exit. These are selected using the left and right arrow keys.

#### Main Menu

The Main Menu presents a list of fields, for example, “PnP Operating System” (selects whether the BIOS or Plug and Play operating system configures Plug and Play devices); “Reset Configuration Data”, “System Time”, “System Date”, “Key Click”, “Key auto-repeat speed” “Delay before auto-repeat” and Numlock at Power-on”. By default the “Reset Configuration Data” item is set to “No”. Selecting “Yes”, will clear the system configuration data.

#### Advanced Menu

The Advanced Menu does not have the same structure as the Main Menu and Power Menu. Instead of presenting a list of fields, it offers a list of sub-menus. The Advanced Menu contains the following sub-menus:

- *Processors, Memory and Cache*. Configures processor, CPU speed, Processor Serial Number, memory controller and cache operations (error correction, shadowing and caching).
- *Floppy Disk Drives*. Enables or disables the on-board floppy disk controller.
- *IDE Devices*. Configures IDE devices. Setting of IDE Primary and Master slave devices, and IDE Secondary Master slave devices. To use both these channels, the Integrated BUS IDE adapter is set to **Both Enabled**.

- *Integrated USB Interface.* Enable or disable the integrated USB (Universal Serial Bus) interface. Setting this option to **Auto** lets the BIOS or PnP operating system configure the device. However, disabling this option leaves the devices disabled by the BIOS, but a PnP operating system can still configure it.
- *Integrated Audio Interface.* Enables or disables the audio interface. Setting this option to **Auto** lets the BIOS or PnP operating system configure the device. Disabling this option frees resources used by the device.
- *Integrated I/O Ports.* Enables or disables the on-board parallel and serial ports at the specified address.
- *Integrated SCSI.* Enables or disables the Option ROM scan, Bus Master and Bus Latency Timer.

## Security

Sub-menus are presented for changing the characteristics and values of the System Administrator Password, User Password, Power-on Password, boot device security and Hardware Protection. The Security Menu contains the following sub-menus:

- *Administrator Password.* This password prevents unauthorized access to the computer's configuration. It can also be used to start the computer when power-on password is set to **Auto**.
- *User Password.* This password can only be set when an administrator password has been set. The User Password prevents unauthorized use of the computer and is used to start the computer when power-on password is set to **Auto**.
- *Power-on Password.* If enabled, a password will be requested on boot.
- *Start from Floppy, Start from CD-ROM and Start from HDD.* These devices can be disabled to prevent unauthorized use to start the computer.
- *Hardware Protection.* The following devices can have their accesses unlocked/locked: floppy disk drives and hard disk boot sector.

## 5 HP BIOS

### HP/NBA BIOS Summary

#### Boot Menu

The QuickBoot Mode option allows the system to skip certain tests while booting. This decreases the time needed to boot the system. From this menu, you can also display the option ROM messages. Enabling this option is recommended when installing an accessory card. It can be disabled when accessory card installation has been completed.

If both AGP and PCI video cards are installed, use the setting to select which will be used as a boot display device. If only one video card is installed, the setting is not used.

Select the order of the devices from which you want the BIOS to attempt to boot the operating system. During POST, if the BIOS is unsuccessful at booting from one device, it will then try the next one on the *Boot Device Priority* list until an operating system is found.

#### Power Menu

This menu allows you to set the standby delay and suspend delay. Standby mode slows down the processor, while the suspend mode saves a maximum of energy. Both these options are only available with Windows 95. For other operating systems, Windows 98 and Windows 2000, use the control panel for similar options

Modem ring enables or disables the system to return to full speed when an IRQ is generated. Network interface enables or disables the system to return to full speed when a specific command is received by the network interface.

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## Updating the System BIOS

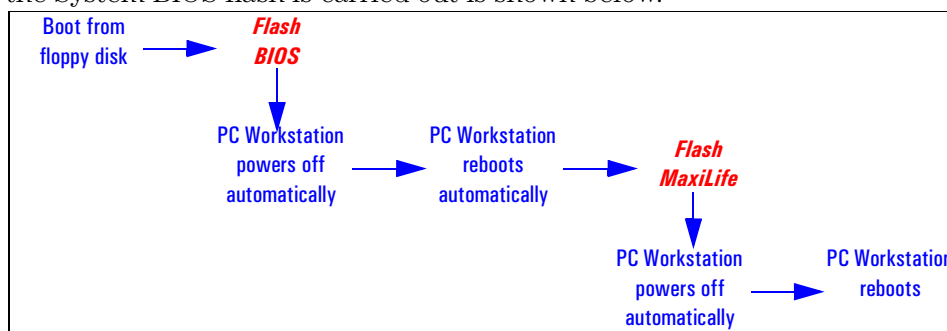
The System BIOS can be updated with the latest BIOS firmware. This can be downloaded from HP's World Wide Web site:

<http://www.hp.com/go/kayaksupport>

then select HP Kayak XU800 PC Workstation.

Instructions on updating the BIOS are supplied with the downloaded BIOS files and a BIOS flash utility (flash.txt).

The BIOS update not only flashes the BIOS, but also updates MaxiLife. How the System BIOS flash is carried out is shown below.



Do not switch off the computer until the system BIOS update procedure has completed, successfully or not, otherwise irrecoverable damage to the ROM may be caused. While updating the flash ROM, the power supply switch and the reset button are disabled to prevent accidental interruption of the flash programming process.

---

## Restoring BIOS Default Settings

Suspected hardware errors may be caused by BIOS and configuration issues. If the BIOS settings are suspected to be wrong, perform the following steps to restore the BIOS to its default setting:

- 1 Press **F2** while the initial "Kayak" logo is displayed immediately after re-starting the PC Workstation to access the *Setup* program.
- 2 Press **F9** to load the default settings from the *Setup* program.
- 3 Set the "Reset Configuration Data" to Yes in the Main menu.  
It is recommended that before you make any modifications to the BIOS you take note of the system setup.

---

## Clearing the CMOS

- 1 Turn off the PC Workstation, disconnect the power cord and data cables, then remove the cover.
- 2 Set the system board switch 4 to the **DOWN** position to clear the CMOS memory.
- 3 Replace the cover, and only reconnect the power cord.
- 4 Reboot the PC Workstation. A message similar to the following will be displayed:

**"Configuration has been cleared.**

**You can now:**

**Switch off the PC Workstation and remove the cover.**

**Reset the "Clear Configuration" switch to OFF (Up).**

**Replace the cover.**

**Switch on the PC Workstation and allow it to startup.**

**To modify the default configuration information:**

**press [F2] when prompted during self-test (POST), to enter  
Setup."**

- 5 Turn off the PC Workstation, disconnect the power cord, and remove the cover.
- 6 Set the system board switch 4 to the **UP** position to retain the configuration.
- 7 Replace the cover, and reconnect the power cord and data cables.
- 8 Switch on the PC Workstation. Run the *Setup* program by pressing **(F2)**. Then press **(F9)**. The CMOS default values will be automatically downloaded and saved.
- 9 Press **(F3)** to save the configuration and exit from the *Setup* program.



---

## Clearing Passwords

To clear the Administrator and User password (for example, Administrator password has been forgotten), perform the following steps:

- 1 Turn off the PC Workstation, disconnect the power cord and data cables, then remove the cover.
- 2 Set the system board switch 3 to the UP position to clear passwords.
- 3 Replace the cover, and only reconnect the power cord.
- 4 Reboot the PC Workstation. A message similar to the following will be displayed:

**"Passwords have been cleared.**

**You can now:**

**Switch off the PC Workstation and remove the cover.**

**Reset the "Clear Password" switch to ON (Down).**

**Replace the cover.**

**Switch on the PC Workstation and allow it to startup.**

**To modify the password setting:**

**press [F2] when prompted during self-test (POST),  
to enter Setup."**

- 5 Turn off the PC Workstation, disconnect the power cord, and remove the cover.
- 6 Set the system board switch 3 to the DOWN position to retain the configuration.
- 7 Replace the cover, and reconnect the power cord and data cables.
- 8 Switch on the PC Workstation. Run the *Setup* program by pressing **(F2)**. Then select the Security menu from the band along the top of the Setup screen.
- 9 Press **(F3)** to save the configuration and exit from the *Setup* program.

---

### Recovering the BIOS (Crisis Mode)

If for some reason the BIOS is corrupted and the standard flash cannot be used, use the BIOS Recovery Mode (exceptional BIOS recovery operation) to restore the BIOS.

The following recovery operation is also documented in the flash.txt file which is supplied with the downloaded BIOS files.

To restore the BIOS:

- 1 Copy the BIOS files on to the floppy disk.
- 2 Rename the file A111xx.rom to **amiboot.rom**.
- 3 Shut down the PC Workstation.
- 4 Power off the PC Workstation and remove the power cord and cables.
- 5 Remove the cover.
- 6 Set switch 1 to the DOWN position.
- 7 Insert the floppy disk into the floppy disk drive.
- 8 Reconnect the power cord and switch on the PC Workstation.
- 9 The PC Workstation boots from the floppy disk, then flashes the BIOS. However, it should be noted that during the flash process, the screen remains blank. MaxiLife will display a message on the LCD panel "RECOVERY MODE".
- 10 The recovery process is finished when there are four beeps.
- 11 Power off the PC Workstation. Remove the floppy disk from the drive. Remove the power cord.
- 12 Set switch 1 back to the UP position.
- 13 Replace the cover, reconnect the power cord, then reboot the PC Workstation.

---

## Adaptec SCSISelect Configuration Utility

The AIC-7892 BIOS includes the SCSISelect configuration utility, which allows you to view and change host adapter settings. SCSISelect also lists the SCSI IDs of devices on the host adapter, formats SCSI disk drives, and checks drives for defects.

### Default Settings

The following tables show the default configuration settings that can be changed. The first table shows the global settings which impact the host adapter; the second table shows the boot device options which allow you to specify the boot device; the third table shows the different advance configuration options; and the fourth table shows the device settings which apply to individual devices.

SCSI BUS Interface Options		
<i>Host Adapter and SCSI Parity Checking Settings</i>	<i>Default Settings</i>	<i>Comments</i>
Host Adapter SCSI ID	7	Each device on the SCSI bus, including the adapter, must have a unique SCSI ID. Allowable IDs are 0 - 15.
SCSI Parity Checking	Enabled	Each adapter verifies the accuracy of data transfer on the SCSI bus.

Boot Device Options		
<i>Boot Target ID and Boot LUN Number Settings</i>	<i>Default Settings</i>	<i>Comments</i>
Boot Target ID	0	To specify a different boot device, choose a SCSI ID 0 - 15. If the boot device has multiple logical units, you must specify the boot LUN, which can be 0 - 7.
Boot LUN Number	0	

Advanced Configuration Options		
<i>Options</i>	<i>Default Settings</i>	<i>Comments</i>
Reset SCSI Bus at IC Initialization	Enabled	BIOS resets the SCSI at POST time (scans the bus for SCSI devices).

## 5 HP BIOS

### Adaptec SCSISelect Configuration Utility

<b>Advanced Configuration Options</b>		
<i>Options</i>	<i>Default Settings</i>	<i>Comments</i>
Extended BIOS Translation for DOS drives > 1 GByte	Enabled	Includes an extended translation scheme that supports disk drives of more than 1 GByte.
Verbose/Silent Mode	Verbose	Displays messages on the screen at POST.
Host Adapter BIOS	Enabled	Controls the state of the BIOS at POST.
Support for Removable Disks Under BIOS as Fixed Disks	Disabled	No removable media drives running under DOS are treated as hard disk drives. Driver software is required because the drives are not controlled by the BIOS.
Display < F6 > message during BIOS Initialization	Enabled	Displays <b>Press F6 for SCSISelect(TM) Utility!</b>
BIOS Support for Bootable CD-ROM	Enabled	Enables booting from a CD-ROM.
BIOS Support for Int 13h Extensions	Enabled	Host adapter BIOS supports Int 13h extensions.
Domain Validation	Disabled	Downgrades the performance while maintaining the integrity of data transmission

<b>SCSI Device Configuration Options</b>		
<i>SCSI Device Options</i>	<i>Default Settings</i>	<i>Comments</i>
SyncTransfer Rate	160	Determines the synchronous data transfer rate that the host adapter will negotiate with the device.
Enable Disconnection	Yes	Determines whether the host adapter allows a SCSI device to disconnect from the SCSI bus (also referred to as Disconnect/Reconnect).
Initiate Wide Negotiation (16-bit adapters only)	Yes	Allows the adapter to initiate wide negotiation with a 16-bit SCSI device.
Send Start unit Command	Yes	Determines whether the host adapter sends the Start Unit command to the SCSI bus.
Enable Write Back Cache	N/C	Allows the BIOS to program the state of the write back cache in the hard disk drive.
BIOS Multiple Lun Support	No	Allows the BIOS to support multiple logical units.
Include in BIOS Scan	Yes	Determines whether the host adapter BIOS supports devices attached to the SCSI bus without the need for device driver software.

### Starting the SCSISelect Configuration Utility

Just after the “*Kayak*” boot screen, press **F6** when the message **Press F6 for SCSISelect(TM) Utility!** is displayed.

---

**NOTE**

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The above message will not be displayed if “*Display <F6> Messages During BIOS Initialization*” has been disabled in the Advanced Configuration Options. The default setting for this option is Enabled.

Follow the on-screen instructions to access the required menu. Any changes made in SCSISelect must be saved and the PC Workstation rebooted for modifications to take affect.

---

## BIOS Addresses

This section provides a summary of the main features of the HP system BIOS. This is software that provides an interface between the computer hardware and the operating system. The procedure for updating the System ROM firmware is described on [page 68](#).

### System Memory Map

Reserved memory used by accessory boards must be located in the area from C8000h to EFFFFh.

0000 0000 - 0000 03FF	Real-mode IDT
0000 0400 - 0000 04FF	BIOS Data Area
0000 0500 - 0009 FC00	Used by Operating System
0009 FC00 - 0009 FFFF	Extended BIOS Data Area
000A_0000 - 000B_ FFFF	Video RAM or SMRAM (not visible unless in SMM)
000C 0000 - 000C 7FFF	Video ROM (VGA ROM)
000C 8000 - 000F FFFF	Adapter ROM, RAM, memory-mapped registers, BIOS
000E 0000-000F FFFF	128 KB BIOS (Flash/Shadow)
0001 0000-000F FFFF	Memory (1 MB to 16 MB)
0010 0000-001F FFFF	Memory (16 MB to 32 MB)
0020 0000-003F FFFF	Memory (32 MB to 64 MB)
0040 0000-007F FFFF	Memory (64 MB to 128 MB)
0080 0000-7FFF FFFF	Memory (128 MB to 2 GB)
FEC0 0000	I/O APIC
FEE0 0000	Local APIC (each CPU)
FFFE 0000-FFFF FFFF	128 KB BIOS (Flash)

## HP I/O Port Map (I/O Addresses Used by the System<sup>1</sup>)

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space, which is not located in system memory space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit registers (called I/O ports) located in the various system components. When installing an accessory board, ensure that the I/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

Default Values for I/O Address Ports	Function
0000 - 000F	DMA controller 1
0020 - 0021	Master interrupt controller
002E - 002F	
0040 - 0043	Timer 1
0060, 0064	Keyboard controller (reset, slow A20)
0061	Port B (speaker, NMI status and control)
0070	Bit 7: NMI mask register
0070 - 0071	RTC and CMOS
0080	Manufacturing port (POST card)
0081 - 0083,	
008F	DMA controller
0092	
00A0 - 00A1	Slave interrupt controller
00C0 - 00DF	DMA controller 2
00F0 - 00FF	Co-processor error
0130 - 013F	
0170 - 0177	ICH (82801AA) bus master IDE controller
01F0 - 01F7	IDE primary channel
0200	
0220 - 0232	
0278 - 027F	
02E8 - 02EF	
02F8 - 02FF	Serial port 2 (COM2)
0330 - 0331	
0372 - 0377	
0378 - 037A	LPT1

1.If configured.

## 5 HP BIOS

### BIOS Addresses

Default Values for I/O Address Ports	Function
0388 - 038B	
03B0 - 03DF	VGA
03E8 - 03EF	
03F0 - 03F5	
03F6	IDE primary channel
03F7	Flexible disk drive controller
03F8 - 03FF	COM1
04D0 - 04D1	System board resources under Windows 95
0678 - 067B	
0778 - 077B	LPT1 ECP
0CF8 - 0CFF	PCI configuration space
8000 -	
8400 -	
8800 -	

### DMA Channel Controllers

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed. “I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration. The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB. The following table summarizes how the DMA channels are allocated.

DMA controller	
Channel	Function
DMA 0	Free
DMA 1	Free
DMA 2	Flexible disk drive controller
DMA 3	LPT ECP
DMA 4	DMA controller
DMA 5	Free
DMA 6	Free
DMA 7	Free



### IRQs Used by the PC Workstation

The IRQ address mappings shown here are for a basic configuration. The resources used by the PC Workstation may vary, depending on which accessory cards are bundled with the PC Workstation. Resources are allocated by the system BIOS or the Plug and Play operating system.

<b>IRQs used by PC Workstation</b>	IRQ0	System timer
	IRQ1	Keyboard controller
	IRQ2	Free
	IRQ3	COM2, COM4
	IRQ4	COM1, COM3
	IRQ5	
	IRQ6	Flexible disk drive controller
	IRQ7	LPT1
	IRQ8	Real-time clock
	IRQ9	
	IRQ10	
	IRQ11	
	IRQ12	Mouse
	IRQ13	Not connected
	IRQ14	Integrated IDE controller (primary)
IRQ15	Integrated IDE controller (secondary)	

**5 HP BIOS**  
BIOS Addresses

## Tests and Error Messages

This chapter describes the MaxiLife firmware test sequences and error messages, the Power-On-Self-Test (POST) routines, which are contained in the computer's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

---

### MaxiLife Test Sequence and Error Messages

When the PC Workstation is turned on (pressing the ON/OFF button), the system initiates the normal startup sequence which is composed of the following steps:

- Basic pre-boot diagnostics
- BIOS launch
- POST phase
- Operating System boot phase

If any errors are detected during the startup sequence, MaxiLife will not necessarily 'freeze' the system. However, some critical hardware errors are fatal to the system and will prevent the system from starting (for example, 'Power' and 'Board PLL' are serious malfunctions that will prevent the CPU from working correctly).

Errors that are not so critical will be detected both during pre-boot diagnostics and POST where the BIOS boot process will abort after beeping. The MaxiLife LCD status panel will display the error. Some errors are only detected during POST sequence, and produce the same abort process.

Finally, while the PC Workstation is working, fan and temperature controls can be reported (for example, a fan error will be reported if a fan cable is not connected). This type of error disappears as soon as the problem is fixed (for example, the fan cable has been reconnected).

The different diagnostics are described below.

## 6 Tests and Error Messages

### MaxiLife Test Sequence and Error Messages

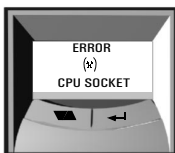
#### Basic Pre-boot Diagnostics

The first diagnostic (called basic pre-boot diagnostics) is run to check the presence of the processor(s) or terminators, VRMs, power supply, CPU Board PLL and memory.

The pre-boot diagnostic tests are run in order of priority with respect to their importance to computer functions.

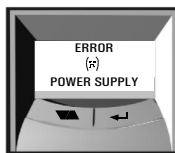
The first detected error displays a message on the LCD status panel. If this happens, one of the following screens could appear.

Presence of processor, processor terminator or VRM



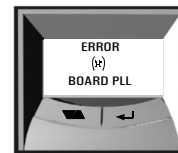
Missing or installed processor or processor terminator

Control of Some Voltages : VRMs, 12V, 3.3V, 1.8V, 2.5V



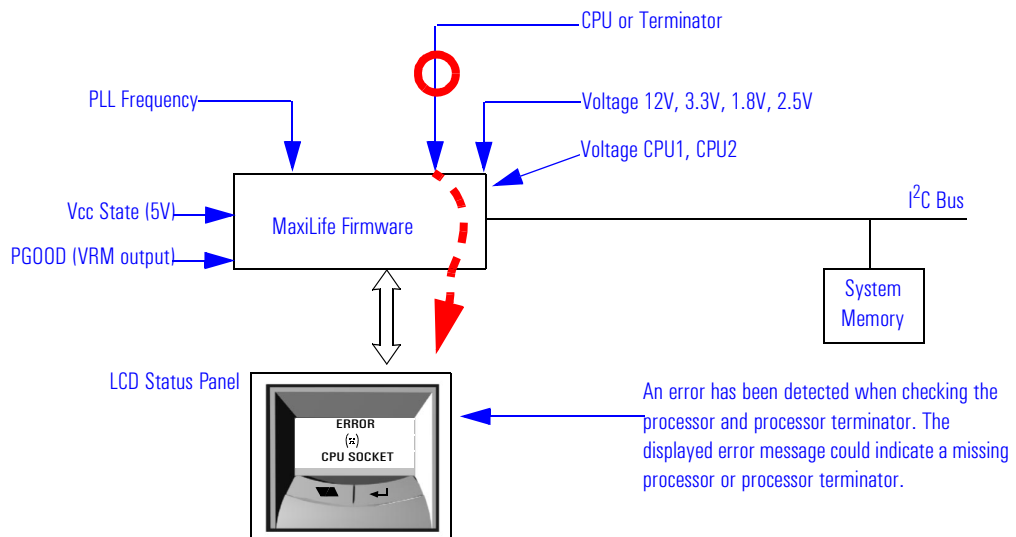
VRM or CPU power supply are not connected. If an Error Power message is displayed, a cause could be that the power supply is not connected, or the VRM is installed with an unpopulated CPU socket (unsupported configuration).

Control of the CPU Board



System Board is not connected, or the system board needs replacing.

The following diagram shows how the Pre-boot Diagnostics works when it encounters an error.

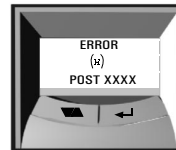


The following table shows the test sequence carried out, the type of error message, and the action to take.

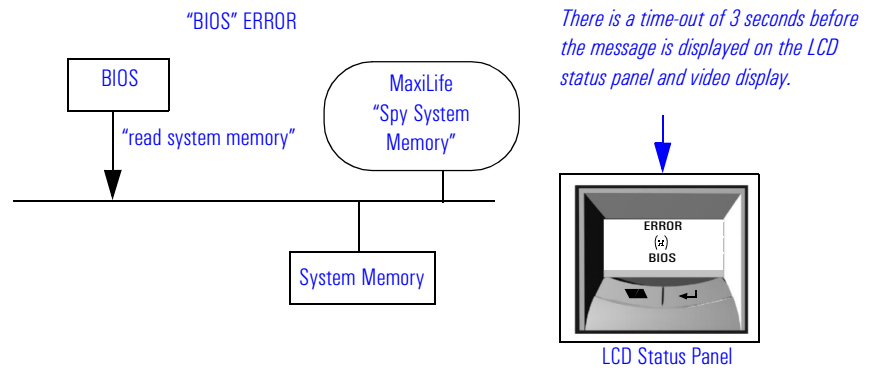
Test	Error Code	Action to Take
Presence of either a processor or processor terminator	CPU SOCKET	Check that the processor(s), processor terminator and VRM are correctly installed.
Control of some voltages: VRMs, 12V, 3.3V, 1.8V, 2.5V	POWER SUPPLY	Check the power supply cable and connectors, VRM and processor.
Check the system board clock generators (PLL).	BOARD PLL	<ol style="list-style-type: none"> <li>1 Check that the system board is connected</li> <li>2 Replace the system board (PLL clock generator).</li> </ol>

### Post Test Sequence and Post Error

In this phase, MaxiLife waits for any error messages that the BIOS may issue. If such an error occurs, then a screen similar to the following example is displayed. The error code that appears on the LCD status panel is the same as the one that appears on the monitor screen. If the POST issues several error codes, only the last one is visible on the LCD status panel.

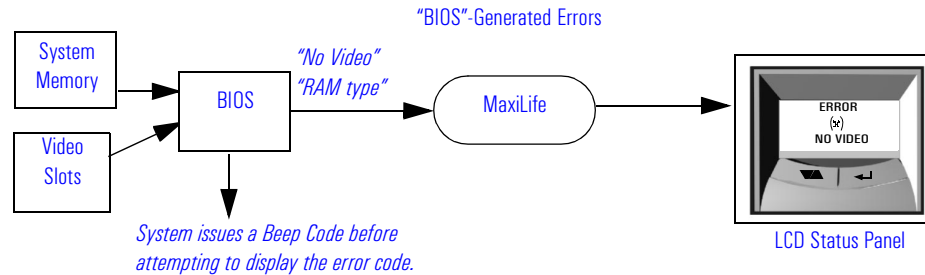


The following diagrams show the different BIOS-generated errors.



## 6 Tests and Error Messages

### MaxiLife Test Sequence and Error Messages



Test	Error Code	Action to Take
Presence of continuity modules in the RIMM sockets	RIMM CONTINUITY	Check that the RDRAM continuity modules are installed
Presence of RDRAM modules	NO RIMM	Install RDRAM modules in the RIMM sockets
Compatibility speed rating of installed RDRAM modules	RIMM SPEED	Check that the installed RDRAM modules have the same speed ratings
presence of installed SDRAM modules	NO DIMM	Check that the SDRAM modules are correctly installed in the DIMM sockets
Presence of installed memory modules in pairs per channel	MEM MISCOMPARE	Check that the RDRAM modules are correctly installed in pairs
Presence of memory modules	MEMORY ERROR	Check that the memory modules are correctly installed
Availability of video controller. It is checked by the BIOS. If an error is detected, it is not a fatal one and the BIOS will continue its execution normally.	NO VIDEO	Check that the video controller is correctly installed  Note: No error is detected if a monitor is not connected to an installed video controller. This is not a fatal error and the BIOS will continue its normal execution.
The BIOS then executes the Power On Self Test (POST) sequence. In this phase, MaxiLife waits for any error messages that the BIOS may issue.	POST XXXX	If the screen is working, you can obtain the meaning of the error by typing "Enter" at the end of the POST.

### Operating System Boot Phase

If no error message has been displayed at this stage of the system startup by the BIOS, the operating system is launched and the LCD status panel will display the system platform and a "smiling icon."

## Run-Time Errors

During the normal usage of the PC Workstation (and at boot), MaxiLife continually monitors vital system parameters. These include: temperature errors, fan malfunctions, power voltage drops, board PLL problems and CPU problems.

If both the fan for disks and the I/O slot are not connected (both are run-time error 1), only the “Fan disk” will be displayed.

Test	Error Code	Action to Take
During normal usage of the PC, HP MaxiLife continually checks vital system parameters. If an error occurs, a message appears on the LCD panel.	FAN CPU	Rear fan, system board, <sup>1</sup> fan cable.
	FAN PCI	PCI fan, PCI cards, system board, fan cable.
	TEMP. CPU	Rear fan, airflow guide, “Airflow Separator” <sup>2</sup> , system board.
	TEMP PCI	PCI fan, airflow guide, “Airflow Separator”, system board, PCI cards.
	TEMP DISK	Rear fan, airflow guide, “Airflow Separator”, disk temperature, sensor, system board.
	POWER ERRORS	Power supply unit, VRM, system board.
	BOARD PLL	Processor(s), system board
	POWER 12V ERROR	Power supply unit has failed. Try the following: <ol style="list-style-type: none"> <li>1 Replace the power supply unit with a known working one</li> <li>2 If the problem persists, replace the system board</li> </ol>
	VCC CPU 1 ERROR	
	VCC CPU 2 ERROR	
	POWER 1.5V ERROR	
	POWER 1.8V ERROR	
	POWER 2.5V ERROR	
POWER 3.3V ERROR		
POWER 5V ERROR		

<sup>1</sup>Special cases: Board PLL = System board needs replacing. CPU error = Reset or power off the system to recover.

<sup>2</sup>A retaining bar holds the airflow guide in place, dividing inside the chassis into two separate areas (processor and PCI slots) for better cooling.

## 6 Tests and Error Messages

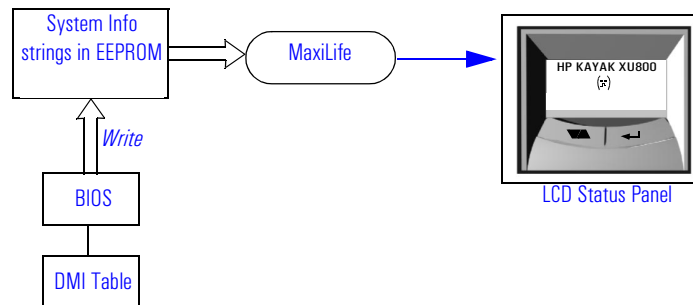
### MaxiLife Test Sequence and Error Messages

#### Main Menu

The main menu is displayed when any of the LCD buttons are pressed (MaxiLife LCD status panel can be accessed even though the PC Workstation is turned off). The Main Menu comprises three sub-menus: System Info, Boot Steps and Diagnostics.

#### System Info

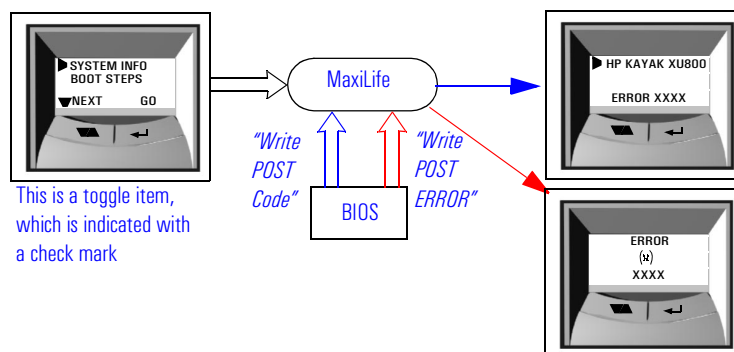
Obtains information from the BIOS and the system's Serial EEPROM from a previously successful boot. This information includes: product name, BIOS version, serial number, number of processors and speed, size of memory for each socket. The following diagram shows how the System Info obtains its information.



#### Boot Steps

Shows the Power-On-Self-Test (POST) codes during the system startup. The POST code is provided by the BIOS and is displayed on the LCD panel as soon as it is available. If the system stops during the startup, the last successful boot step POST code is displayed on the LCD. When Boot Steps is selected, the POST step will be shown on the LCD status panel during the subsequent boot processes.

To ensure that MaxiLife is ready to display the first POST codes as soon as possible, the Pre-boot diagnostics are not executed when the system is booted with the Boot Steps option selected. The following diagram shows how Boot Steps obtains its information from the BIOS, and then displays a POST error if needed.





## Diagnostics

Runs a set of diagnostics assessing the system's components. Results of the tests are displayed on the LCD status panel, one after another, when the LCD ▼▲ buttons are pressed.

It is possible to cancel the diagnostic process and return to the previous state by pressing the LCD key labelled "Back". When "OK" is selected, the main power supply is started but the PC Workstation is not allowed to do a normal boot. The purpose of this is to allow only those devices that can be tested to answer the diagnostic request from MaxiLife.

Components are tested in sequence when the "Next" button is pressed. When they have all been checked, a diagnostic screen is shown. Depending on the result of the diagnostics, the screen could indicate either: OK or FAIL.

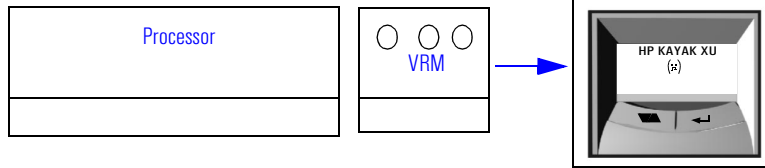
At the end of the test, you can exit the diagnostic mode by pressing the ← LCD button.

## 6 Tests and Error Messages

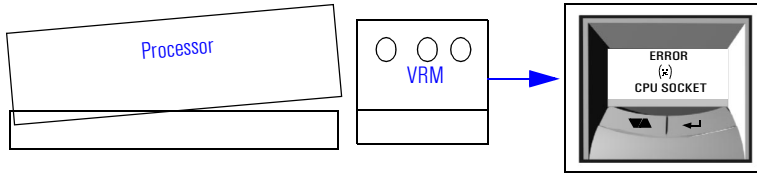
### MaxiLife Test Sequence and Error Messages

#### Typical Diag Error Messages

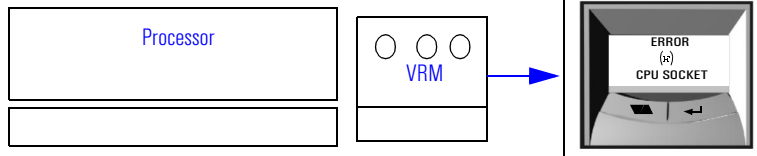
*When the Processor and VRM are correctly installed, the "smiling icon" is shown on the LCD status panel.*



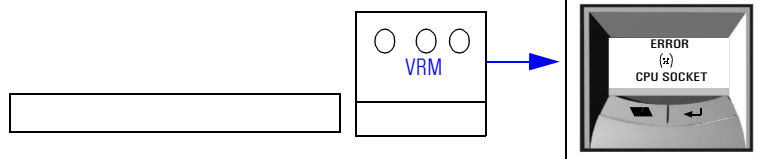
*If the Processor has only been partly inserted in the processor slot, then the displayed message will indicate a CPU socket error.*



*The Processor has not been inserted correctly in the processor slot. The displayed message will indicate a CPU socket error.*



*There is no installed Processor. However, the VRM is correctly installed. The displayed message will indicate a Power error.*



#### For More Information About MaxiLife

Refer to the online *Troubleshooting Guide* for more information about this diagnostics utility at the HP World Wide Web site:

<http://www.hp.com/go/kayaksupport>.

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## Order in Which POST Tests Are Performed

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters.

The POST starts by displaying a graphic screen of the HP PC Workstation's logo when the PC Workstation is restarted. If you wish to view the POST details, press **[Esc]** to get the HP Summary Screen.

If the POST detects an error, the error message is displayed inside a view system errors screen, in which the error message utility (EMU) not only displays the error diagnosis, but the suggestions for corrective action (refer to [page 123](#) for a brief summary). Error codes are no longer displayed on MaxiLife LCD panel.

Devices such as memory and newly installed hard disks, are configured automatically. The user is not requested to confirm the change. Newly removed hard disks are detected, and the user is prompted to confirm the new configuration by pressing **[F4]**. Note, though, that the POST does not detect when a hard disk drive has been otherwise changed.

During the POST, the BIOS and other ROM data are copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

### An example of an Error Code Message

This example explains the different coding messages that appear in the lower left corner of the screen when the POST detects an error during startup.

For example, if the error 0101 - 52 is displayed.

0101 - Post Error Code failure. This error code is accompanied by a short message. For this example, the message "keyboard error" is displayed on the screen and MaxiLife LCD panel.

A table listing the error codes, causes and symptoms is on [page 124](#).

52 - Post Checkpoint Code. This checkpoint code indicates that a test has failed at this stage of the POST. If the "Boot Step" option has been validated in MaxiLife, then Post Checkpoint Codes (in this example, 52) will be reported to the MaxiLife.

## 6 Tests and Error Messages

### Order in Which POST Tests Are Performed

A Check Point Code allows you to follow the POST schedule on the MaxiLife LCD panel. To achieve this, you first need to select the “Boot Step” option in the “Service” menu of MaxiLife.

The following table lists the POST checkpoint codes written at the start of each test and listed in order of execution.

<b>Checkpoint Code</b>	<b>POST Routine Description (A Check Point Code is NOT an error code or error number)</b>
<b>Uncompressed Initialization Codes</b>	
D0h	NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode.
D3h	Starting Memory sizing.
D4h	Returning to real mode. Executing any patches and setting the stack.
D5h	Passing control to the uncompressed code shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is segment 0. Next, checking if < Ctrl > < Home > was pressed and verifying the system BIOS checksum.  If either < Ctrl > < Home > was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h.  Otherwise, going to checkpoint code D7h.
D7h	Passing control to the interface module.
D8h	Main system BIOS runtime code will be decompressed.
D9h	Passing control to the main system BIOS in shadow RAM.
<b>Bootblock Recovery Codes</b>	
E0h	Onboard floppy disk driver controller is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table.
E2h	Initializing the DMA and Interrupt controllers.
E6h	Enabling the floppy disk drive controller, Timer IRQs and internal cache memory.

Checkpoint Code	POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)
EDh	Initializing the floppy disk drive.
EEh	Looking for a floppy disk in drive A: Reading the first sector of the floppy disk.
EFh	A read error occurred while reading the floppy disk drive A:.
F0h	Searching for the AMIBOOT.ROM file for the root directory.
F1h	AMIBOOT.ROM file is not found in the root directory.
F2h	Reading and analyzing the floppy disk FAT to find clusters occupied by the AMIBOOT.ROM file.
F3h	Reading the AMIBOOT.ROM file, cluster by cluster.
F4h	AMIBOOT file is not the correct size.
F5h	Disabling internal cache memory.
FBh	Detecting the type of flash ROM.
FCh	Erasing the flash BIOS.
FDh	Programming the flash BIOS.
FFh	Flash PROM programming was successful. Restarting the system BIOS.
<b>Uncompressed Initialization Codes</b>	
<i>The following routine checkpoint codes are listed in order of execution. These codes are uncompressed in F000h shadow RAM.</i>	
03h	Disable Non-Maskable Interrupt (NMI)
05h	BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code.
07h	Initializing processor and the processor data area.
08h	CMOS checksum calculation performed.
0Bh	Performing any required initialization before the keyboard BAT command is issued.
0Ch	Keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.

## 6 Tests and Error Messages

### Order in Which POST Tests Are Performed

<b>Checkpoint Code</b>	<b>POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)</b>
0Eh	Keyboard controller BAT command result has been verified. Next performing any necessary initialization after the keyboard controller BAT command test.
0Fh	Keyboard command byte is then written.
10h	Issuing the Pin 23 and 24 blocking and unblocking commands.
11h	Checking if the < End > or < Ins > keys were pressed during power-on. Initializing CMOS RAM if the <i>Initialize CMOS RAM in every boot AMIBIOS POST</i> option was set in AMIBCP or the < End > key was pressed.
12h	Disabling DMA controllers 1 and 2, and Interrupt controllers 1 and 2.
13h	Video display has been disabled. Port B has been initialized. Then, initializing the chipset.
14h	8254 timer initialization.
19h	Initializing memory refresh test.
1Ah	memory refresh line is toggling. Checking the 15 second on/off time.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature. Making the BIOS code segment writable and performing any necessary configuration before initialization the interrupt vectors.
24h	Configuration required before Interrupt vector initialization has completed. Then Interrupt vector initialization begins.
25h	Clearing the password if the POST DIAG switch is on.
27h	Setting video mode.
28h	Video ROM performs any required configuration before the video ROM test.
2Ah	System bus initialization, static, output devices, if present.
2Bh	Video ROM performs any required configuration before testing.
2Ch	All necessary processing before passing control to the Video ROM is completed. Video ROM is searched, then control passed on to it.
2Dh	Video ROM returns control to the BIOS POST. Performing any required processing after the video
2Eh	If the EGA/VGA controller is not found, performing the display memory read/write test.
2Fh	The EGA/VGA controller was not found. The display memory read/write test begins.

Checkpoint Code	POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)
30h	Display memory read/write test passed. Looking for retrace checking.
31h	Display memory read/write test or retrace failed. Performing the alternate display retrace checking.
32h	Alternate display memory read/write test passed. Looking for alternate display retrace checking.
34h	Video display checking is complete. Setting the display mode.
37h	Display mode is set. Displaying the display mode text.
38h	Initializing the bus input, IPL, and if present and general devices.
39h	Displaying the bus initialization errors.
3Ah	New cursor position has been read and saved. Displaying the <i>Hit</i> < DEL > message.
40h	Preparing the descriptor tables.
42h	Descriptor tables are prepared. Entering protected mode for the memory test.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wrap-around at 0:0.
45h	Data initialized. Checking for memory wrap-around at 0:0 and finding total system memory size.
47h	Memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory
48h	Patterns written in base memory. Determining the amount of memory below 1 MB.
49h	Amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB.
4Bh	Amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset. If this is a power on situation, going to checkpoint 4Eh.
4Ch	Memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB.
4Dh	Memory above 1 MB has been cleared via a soft reset. Saving the memory size. Going to checkpoint 52h.
4Eh	Memory test started, but not as the result of the soft reset. Displaying the first 64 KB memory size.

## 6 Tests and Error Messages

### Order in Which POST Tests Are Performed

<b>Checkpoint Code</b>	<b>POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)</b>
50h	Memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing.
51h	Memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB.
52h	Memory above 1 MB has been tested and initialized. Saving the memory size information.
53h	Memory size information and CPU registers are saved. Entering real mode.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI.
57h	The A20 address line, parity, and the NMI disabled. Adjusting the memory size depending on relocation and shadowing.
58h	Memory size was adjusted for relocation and shadowing. Clearing the <i>Hit</i> <DEL> message.
59h	The <i>Hit</i> <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and Interrupt controller test.
60h	DMA page register test passed. Performing the DMA controller 1 base register test.
62h	DMA controller 1 base register test passed. Performing the DMA controller 2 base register test.
65h	DMA controller 2 base register test passed. Programming DMA controllers 1 and 2.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller.
62h	Test extended memory address lines
7Fh	Extended NMI source enabling is in progress.
80h	Keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command.
81h	Keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command.
82h	Keyboard controller interface test completed. Writing the command byte and initializing the circular buffer.
83h	Command byte was written and global data initialization has completed. Checking for a locked key.
84h	Locked key checking is over. Checking for memory size mismatch with CMOS RAM data.



<b>Checkpoint Code</b>	<b>POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)</b>
85h	Memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup.
86h	Password was checked. Performing any required programming before WINBIOS Setup.
87h	Programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup.
89h	Programming after WINBIOS Setup has completed. Display the power on screen message.
8Bh	First screen message has been displayed. The < WAIT... > message is displayed. Performing PS/2 mouse check and extended BIOS data area allocation check.
8Ch	Programming the WINBIOS Setup options.
8Dh	WINBIOS Setup options are programmed. Resetting the hard disk drive controller.
8Fh	Hard disk drive controller has been reset. Configuring the floppy disk drive controller.
91h	Floppy disk drive controller has been configured. Configuring the hard disk drive controller.
95h	Initializing the bus option ROMs from C800.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM is then checked.
98h	Adaptor ROM has control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer bus address.
9Ah	Set the timer and printer bus address. Setting the RS-232 bus address.
9Bh	Returned after setting the RS-232 bus address. Performing any required initialization before the co-processor test.
9Ch	Required initialization before the co-processor test is over. Initializing the co-processor.
9Dh	Co-processor initialized. Performing any required initialization after the co-processor test.
9Eh	Initialization after the co-processor test is complete. Checking the extended keyboard IDn and Num Lock key. Issuing the keyboard ID command.

## 6 Tests and Error Messages

### Order in Which POST Tests Are Performed

<b>Checkpoint Code</b>	<b>POST Routine Description (Continued) (A Check Point Code is NOT an error code or error number)</b>
A2h	Displaying any soft key errors.
A3h	Soft error display has completed; Setting the keyboard typematic rate.
A4h	Keyboard typematic rate is set. Programming the memory wait states.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000h.
A8h	Initialization before passing control to the adaptor ROM at E000h
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000h option ROM had control.
AAh	Initialization after E000h option ROM control has completed. Displaying the system configuration.
ABh	Building the multi-processor table, if necessary.
ACh	Uncompressing the DMI table data and initializing DMI POST.
B0h	System configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific area is done. Passing control to INT 19h boot loader.

---

## Error Message Summary

The Error Message Utility or EMU (.COM application written in C language) is to provide full screen online help messages (localized) on most common POST errors. In the event of an error generated in POST (Power-On-Self-Test) during the boot process, there are two beeps, then the Error Setup Manager gives access to one or more detected errors. For each error, a specific message is displayed on the monitor screen.

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### NOTE

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If the monitor is not available, a short error message is displayed on the MaxiLife LCD panel.

All errors detected by the POST have an associated EMU message. The following examples give the different types of error categories.

<b>Category #1:</b>	If an error can be bypassed with <F1> or solved through Setup, the POST should prompt:
ERROR	
<b>0070</b>	CPU Terminator Card Error
<b>Press &lt; Enter &gt; to view more information about error<sup>1</sup></b>	
<b>&lt; F1 = Continue &gt;</b>	

<sup>1.</sup> Intervention is required. For example, install a CPU Terminator Card in the vacant processor socket.

<b>Category #2:</b>	If the error is only a warning (i.e. key stuck), the POST should prompt:
WARNING	
<b>00100</b>	Keyboard Warning <sup>1</sup>

<sup>1.</sup> Warning message followed by a short timeout period. Then the system continues to boot without any required intervention.

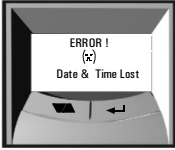
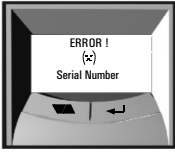
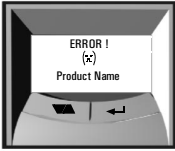
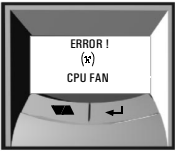
<b>Category #3:</b>	If the error is serious, the POST should prompt:
<b>00xx</b>	The BIOS has detected a serious problem that prevents your PC from booting
<b>Press &lt; Enter &gt; to view more information about error</b>	
<b>&lt; F1 = Continue &gt; , &lt; F2 = Fix &gt;</b>	

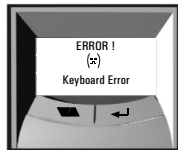

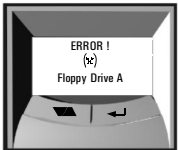
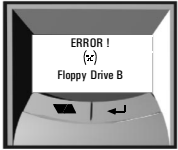
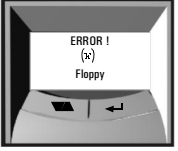
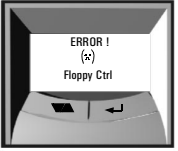
## 6 Tests and Error Messages

### Error Message Summary

The following table lists the error codes, causes and symptoms, and the accompanying short messages that are displayed in the upper left corner of the screen.

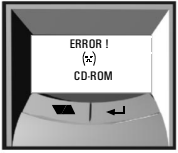
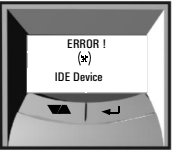
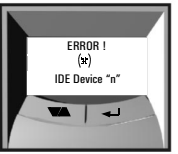
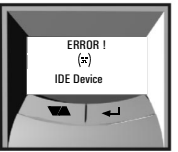
Also shown are the corresponding MaxiLife messages (where available) that are displayed on the LCD panel.

Code #	Cause / Symptom	Short message (US)	Associated MaxiLife LCD message
0000h	Any POST error that is not listed below	System error	
0010h	CMOS Checksum error	Incorrect CMOS Checksum	
0011h	Date and Time (CMOS backed up from SE2P)	Date and Time Lost	
0012h	PC configuration lost (both SE2P and CMOS lost)	Incorrect PC Configuration	
0021h	Any POST error regarding an external PCI card issue	PCI Error	
0040h	Serial number corrupted (bad checksum or null #)	Invalid PC Serial Number	
0041	Product flag not initialized or bad	Invalid Internal product type	
0050h	Fan not connected (according to CPU)	Fan Not Connected	

Code #	Cause / Symptom	Short message (US)	Associated MaxiLife LCD message
0100h	Keyboard stuck key	Keyboard Error	
0101h	Keyboard self-test failure	Keyboard Error	
0102h	Keyboard controller I/O access failure	Keyboard Error	
0103h	Keyboard not connected	Keyboard Not Connected	
0108h	Keyboard and Mouse connectors reversed	Keyboard and Mouse Error	
0105h	Mouse self-test failure	Mouse Error	
0106h	Mouse not detected (but configured in CMOS)	Mouse Error	
0300h	Floppy A: self-test failure	Flexible Disk Drive A Error	
0301h	Floppy B: self-test failure	Flexible Disk Drive B Error	
0305h	Floppy A: plugged on Floppy B: connector	Flexible Disk Drive Error	
0306h	General failure on floppy controller	Flexible Disk Drive Error	
0307h	Conflict on floppy disk controller	Flexible Disk Drive Error	

## 6 Tests and Error Messages

### Error Message Summary

Code #	Cause / Symptom	Short message (US)	Associated MaxiLife LCD message
0400h	CD-ROM test failure	CD-ROM Error	
0500h	General failure on HDD onboard primary ctrl	IDE Device Error	
0501h	General failure on HDD onboard secondary ctrl	IDE Device Error	
0510h	HDD # 0 self-test error	IDE Device # 0 Error	
0511h	HDD # 1 self-test error	IDE Device # 1 Error	
0512h	HDD # 2 self-test error	IDE Device # 2 Error	
0513h	HDD # 3 self-test error	IDE Device # 3 Error	
0530h	Found a drive on slave connector only (primary)	IDE Device Error	
0531h	Found a drive on slave connector only (secondary)	IDE Device Error	
0540h	Conflict on hard disk controller	IDE Device Error	
0800h	Found lower cache size than configured	System Cache Error	

The following table summarizes the most significant of the problems that can be reported.

Message	Explanation or Suggestions for Corrective Action
Operating system not found or all devices have been checked and no operating system has been found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by POST. Check that your boot device is enabled on the Setup Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD type "Auto" parameters.
Resource Allocation Conflict -PCI device 0079 on system board	Clear CMOS.
Video Plug and Play interrupted or failed. Re-enable in Setup and try again	You may have powered your computer Off/On too quickly and the computer turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run Setup for configuration.
No message, system "hangs"	Check that the main memory modules are correctly set in their sockets.
Other	An error message may be displayed and the computer may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the computer is in Time-out Mode. After Time-out, run Setup to check the configuration.

## Beep Codes

If an error occurs during the POST, which prevents the PC Workstation from starting, and before the display device has been initialized, a series of beep codes are issued. Beep codes indicate that a fatal error has occurred and can be reported one after another if there is more than one detected error. In this case, the first detected error is the most important.

## 6 Tests and Error Messages

### Error Message Summary

These codes are useful for identifying the error when the system is unable to display the error message.

Number of Beeps	Description	Action to Take...
1	The memory refresh circuitry is faulty.	Check that: <ul style="list-style-type: none"><li>• Memory is installed correctly.</li><li>• Correct memory modules are being used.</li></ul> If the error still occurs, replace the memory.
2	Parity error in the base memory (the first 64 KB block) of memory.	
3	Memory error.	
4	Clock error.	<ul style="list-style-type: none"><li>• Check that the system board is correctly cabled (power cables, processor and terminator).</li></ul> If the error still occurs, replace the system board.
5	Processor test error.	Check that: <ul style="list-style-type: none"><li>• Processor is correctly installed.</li><li>• Termination card installed in processor slot 2 in a single processor system.</li></ul> If the error still occurs, replace: <ol style="list-style-type: none"><li>1 Processor.</li><li>2 System board.</li></ol>
6	Input/Output (I/O) error.	<ul style="list-style-type: none"><li>• Keyboard is connected.</li><li>• PCI card is installed correctly.</li><li>• Termination card installed in processor slot 2 in a single processor system.</li></ul>
7	The processor on the system board generated an error.	<ul style="list-style-type: none"><li>• There is an installed processor(s).</li><li>• Processor(s) is correctly installed in the processor slot(s).</li><li>• Two installed processors have the same cache size (256 k).</li><li>• Termination card is installed in processor slot 2 in a single processor system.</li><li>• VRM is installed in the VRM socket in a dual processor system.</li></ul> If the error still occurs, replace the system board.
8	The system video card is either missing or faulty.	This is not a fatal error. Check that the video card is correctly installed and cabled. If missing, install the video card. If the error still occurs, replace it with a known working video card.



Number of Beeps	Description	Action to Take...
9	The BIOS Checksum value does not match the value encoded in the BIOS.	Perform the following actions in this order: <ol style="list-style-type: none"> <li>1 Press <b>F2</b> to enter the <i>Setup</i> program, then <b>F9</b> to load the default BIOS settings.</li> <li>2 Clear the CMOS. Refer to <a href="#">page 96</a> for instructions.</li> <li>3 Flash the BIOS. Refer to <a href="#">page 95</a> for instructions on how to update the BIOS.</li> </ol> If the error still occurs, replace the system board.
10	The CMOS RAM has failed.	Perform the following actions in this order: <ol style="list-style-type: none"> <li>1 Press <b>F2</b> to enter the <i>Setup</i> program, then <b>F9</b> to load the default BIOS settings.</li> <li>2 Clear the CMOS. Refer to <a href="#">page 96</a> for instructions.</li> <li>3 Flash the BIOS. Refer to <a href="#">page 95</a> for instructions on how to update the BIOS.</li> </ol> If the error still occurs, replace the system board.
11	The cache memory test failed.	Replace the processor(s).

## 6 Tests and Error Messages

Error Message Summary

## Connectors and Sockets

### IDE Drive Connectors

IDE Connectors			
Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HDO	18	HD15
19	Ground 7	20	orientation key
21	DMARQ	22	Ground 2
23	DIOW#	24	Ground 3
25	DIOR#	26	Ground 4
27	IORDY	28	CSEL
29	DMACK#	30	Ground 5
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS1FX#	38	CS3FX#
39	DASP#	40	Ground 6

Flexible Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSELO#
13	Ground	14	DRSEL1#
15	Ground	16	DTENO#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRKO#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

### Battery Pinouts

Battery Connections	
Pin	Signal
1	GROUND
2	VBAT1
3	VBAT2

Battery Connections	
Pin	Signal
1	VBAT1
2	GROUND

## VRM

VRM			
Pin	Signal	Pin	Signal
A1	5Vin_5	B1	5Vin_2
A2	5Vin_4	B2	5Vin_1
A3	5Vin_3	B3	5Vin_0
A4	12Vin_1	B4	12Vin_0
A5	12Vin_2	B5	SENSE
A6	ISHARE	B6	OUTEN
A7	VID0	B7	VID1
A8	VID2	B8	VID3
A9	VID4	B9	PWRGOOD
A10	VCCP10	B10	GND0
A11	GND5	B11	VCCP4
A12	VCCP9	B12	GND10
A13	GND4	B13	VCCP3
A14	VCCP8	B14	GND9
A15	GND3	B15	VCCP2
A16	VCCP7	B16	GND8
A17	GND2	B17	VCCP1
A18	VCCP6	B18	GND7
A19	GND1	B19	VCCP0
A20	VCCP5	B20	GND6

## SCSI Connectors

SCSI Connector							
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+SCDBI2	2	+SCDBI3	35	-SCDBI2	36	-SCDBI3
3	+SCDBI4	4	+SCDBI5	37	-SCDBI4	38	-SCDBI5
5	+SCDBP1	6	+SCDB0	39	-SCDBP1	40	-SCDB0
7	+SCDB1	8	+SCDB2	41	-SCDB1	42	-SCDB2
9	+SCDB3	10	+SCDB4	43	-SCDB3	44	-SCDB4
11	+SCDB5	12	+SCDB6	45	-SCDB5	46	-SCDB6
13	+SCDB7	14	+SCDB8	47	-SCDB7	48	-SCDB8
15	Ground0	16	DiffSenGround	49	Ground3	50	INT_DEV
17	TERMPWR0	18	TERMPWR1	51	TERMPWR2	52	TERMPWR3
19	RESERVED2	20	Ground1	53	RESERVED1	54	Ground5
21	+ATN	22	Ground2	55	-ATN	56	Ground6
23	+BSY	24	+ACK	57	-BSY	58	-ACK
25	+RST	26	MSG	59	-RST	60	-MSG
27	+SEL	28	+C_D	61	-SEL	62	-C_D
29	+REQ	30	+I_O	63	-REQ	64	-I_O
31	+SCDB8	32	+SCDB9	65	-SCDB8	66	-SCDB9
33	+SCDB10	34	+SCDB11	67	-SCDB10	68	-SCDB11

## Additional SCSI LED Connector

Additional SCSI LED Connector (4-pin)	
Pin	Signal
1	Not used
2	LED Out
3	LED Out
4	Not used

Power Supply Connector  
(20-pin) and  
Aux Power Connector

Power Supply Connector for System Board (20-pin)			
Pin	Signal	Pin	Signal
11	3V3_MAINSENSE	1	3V3_2
12	12V_NEG	2	3V3_3
13	GROUND_1	3	GROUND2
14	_PSON	4	5V_1
15	GROUND3	5	GROUND4
16	GROUND5	6	5V_2
17	GROUND6	7	GROUND7
18	5V_NEG	8	PWOK
19	5V_3	9	5VSB
20	5V_4	10	12V

Aux. Power Connector	
Pin	Signal
1	GROUND1
2	GROUND2
3	GROUND3
4	3V3_1
5	3V3_2
6	5V

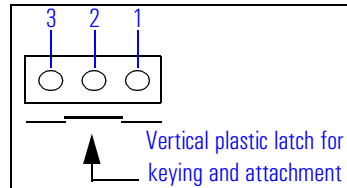
Wake On LAN  
Connector

Wake On LAN (WOL)	
Pin	Signal
1	5V STDBY
2	Ground
3	LAN_WAKE

Rear Fan Connector

Fan Connector	
Pin	Signal
1	Ground
2	12V Power
3	Sense

### PCI Fan Connector



Fan Connector	
Pin	Signal
1	Sense
2	+ 12 V Power (or less, depending on desired fan speed)
3	Ground

### Status Panel and Intrusion

Status Panel			
Pin	Signal	Pin	Signal
1	B1_LCD1	2	B1_LCD2
3	Ground	4	PWR_LED_A
5	HDD_LED_K	6	BACKLIGHT
7	ON_OFF	8	RED-LED_A
9	GROUND2	10	HDD_LED_A
11	_RESET	12	SDA
13	VSTDBY_3V	14	SCL

Intrusion	
Pin	Signal
4	CLOSE
3	COMMON
1	OPEN

### Hard Disk Drive Temperature Connector

HDD Temperature	
Pin	Signal
1	3V3
2	SENSE
4	Ground

## 7 Connectors and Sockets

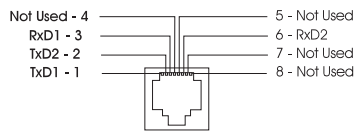
### VGA DB15 Connector

VGA DB Connector Pins		
Pin	Standard VGA	DDC2B
1	Analog RED	Analog RED
2	Analog GREEN	Analog GREEN
3	Analog BLUE	Analog BLUE
4	Monitor ID2	Monitor ID2
5	n/c	DDC return
6	Analog RED return	Analog RED
7	Analog GREEN return	Analog GREEN
8	Analog BLUE return	Analog BLUE
9	n/c	V <sub>CC</sub> supply (optional)
10	Digital ground	Digital ground
11	Monitor ID 0	Monitor ID 0
12	Monitor ID 1	Data:SDA
13	HSYNC	HSYNC
14	VSYNC	VSYNC
15	n/c	Clock:SCL

### LCD Panel

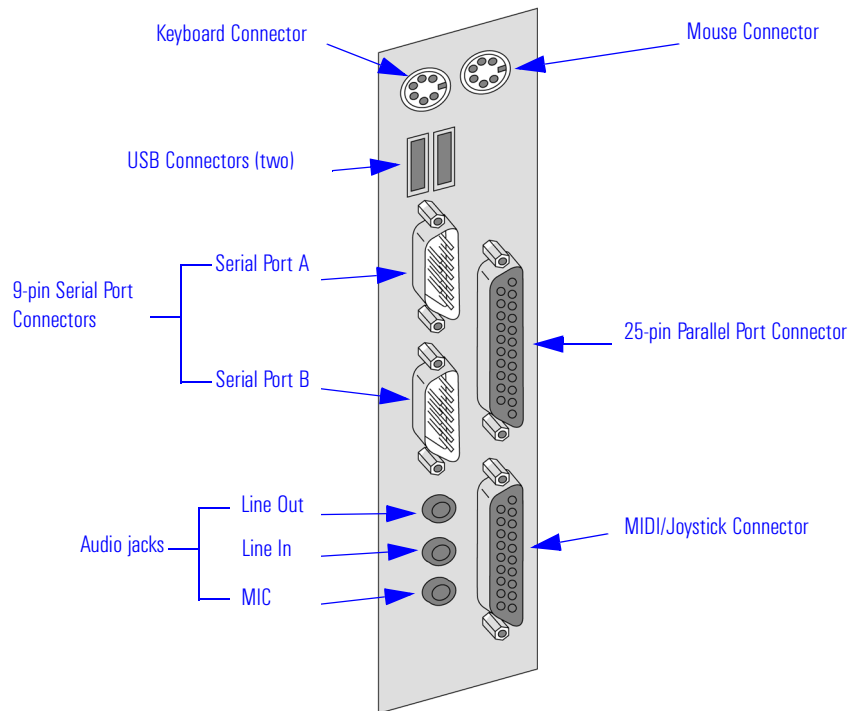
LCD Panel			
Pin	Signal	Pin	Signal
1	SCL_5V	2	VSTDBY 5V
3	SDA_5V	4	BT_LCD 1
5	not connected	6	BT_LCD 2
7	RX_BB	8	TX_BB
9	Ground	10	Ground

### Ethernet UTP Connector

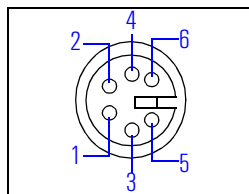




## Rear Panel Socket Pin Layouts



### Keyboard (left) and Mouse (right) Connectors

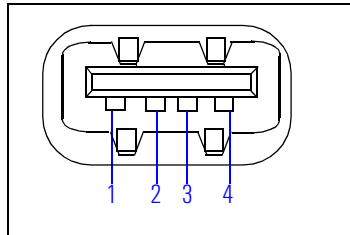


Keyboard and Mouse Connectors			
Pin	Signal	Pin	Signal
1	Data	2	Not Used
3	Ground	4	+5 V dc
5	Clock	6	Not Used

## 7 Connectors and Sockets

### Rear Panel Socket Pin Layouts

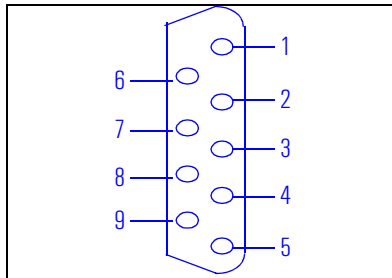
**USB Stacked Connector** The below USB graphic and pinout table is for a USB connector. However, the information is also valid for a USB Stacked Connector.



USB Stacked Connector	
Pin	Signal
1	VBus
2	D-
3	D+
4	GND
Shell	Shield

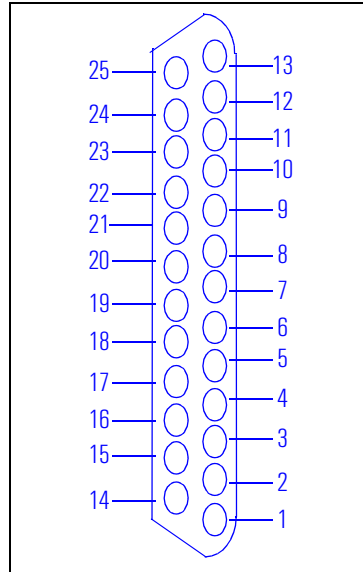
### Serial Port A (top) and Serial Port B (bottom) Connectors

Even though the below graphic and pinout table is for one connector, the information is valid for both the Serial Port A and Serial Port B Connectors.



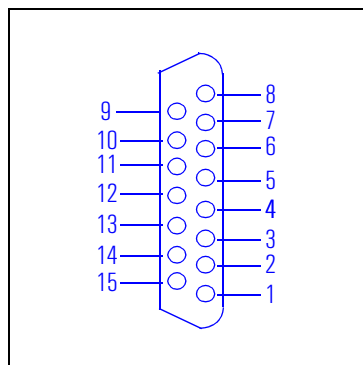
9-pin Serial Port Connector			
Pin	Signal	Pin	Signal
		1	(DCD) CF
6	(DSR) CC	2	(RD) BB
7	(RTS) CA	3	(TD) BA
8	(CTS) CB	4	(DTR) CD
9	(R) CE	5	(GND) AB

## 25-pin Parallel Connector



25-pin Parallel Connector			
Pin	Signal	Pin	Signal
		13	SLCT
25	Ground	12	PE
24	Ground	11	BUSY
23	Ground	10	ACK
22	Ground	9	D7
21	Ground	8	D6
20	Ground	7	D5
19	Ground	6	D4
18	Ground	5	D3
17	SLIN	4	D2
16	INIT	3	D1
15	ERROR	2	D0
14	AUTO-FD	1	Strobe

## MIDI/Joystick Connector



MIDI/Joystick Connector			
Pin	Signal	Pin	Signal
		8	+5 V
9	+5 V	7	A-2
10	B-1	6	A-Y
11	B-X	5	Ground
12	MIDI-OUT	4	Ground
13	B-Y	3	A-X
14	B-2	2	A-1
15	MIDI-IN	1	+5 V

## External Audio Jacks

On the PC Workstation there is a Line In jack, Line Out jack and Mic In jack located on the rear panel. These external jacks are standard connectors.

## 7 Connectors and Sockets

### Rear Panel Socket Pin Layouts